



# SPN68T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN68T10 is the N-Channel enhancement mode power field effect transistor which is produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

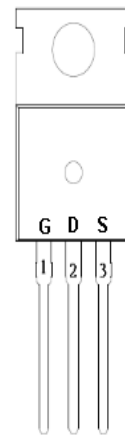
- ◆ 100V/68A,  $R_{DS(ON)}=14m\Omega@V_{GS}=10V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L and TO-252-2L package design

### APPLICATIONS

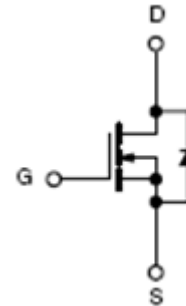
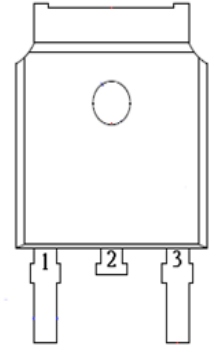
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

### PIN CONFIGURATION

TO-220-3L



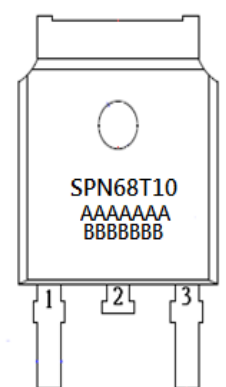
TO-252-2L



### PART MARKING



A : Lot Code  
B : Date Code



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B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN68T10T220TGB	TO-220-3L	SPN68T10
SPN68T10T252RGB	TO-252-2L	SPN68T10

※ SPN68T10T220TGB : Tube ; Pb – Free ; Halogen – Free

※ SPN68T10T252RGB : Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	100	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(Silicon Limited)	I <sub>D</sub>	T <sub>C</sub> =25°C	75
		T <sub>C</sub> =70°C	60
Pulsed Drain Current	I <sub>DM</sub>	301	A
Power Dissipation@ T <sub>C</sub> =25°C	P <sub>D</sub>	166.7	W
Avalanche Energy with Single Pulse ( T <sub>J</sub> =25°C , L=0.1mH , I <sub>AS</sub> =15A , V <sub>DD</sub> =25V , V <sub>GS</sub> =10V)	E <sub>AS</sub>	113	mJ
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Case (TO-220-3L)	R <sub>θJC</sub>	1.2	°C/W
Thermal Resistance-Junction to Case (TO-252-2L)	R <sub>θJC</sub>	1.35	°C/W

#### Note :

The maximum current rating is package limited at 120A for TO-220-3L

The maximum current rating is package limited at 70A for TO-252-2L



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

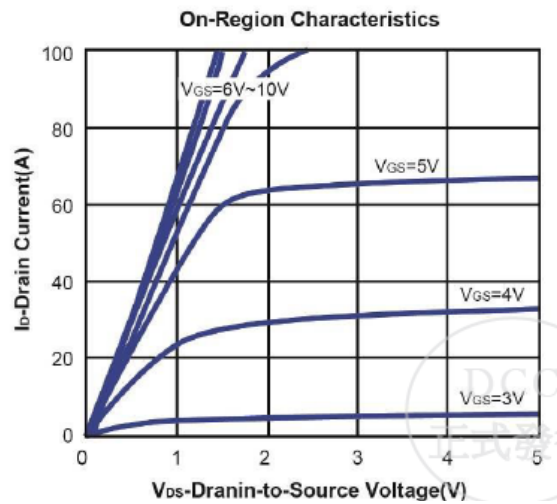
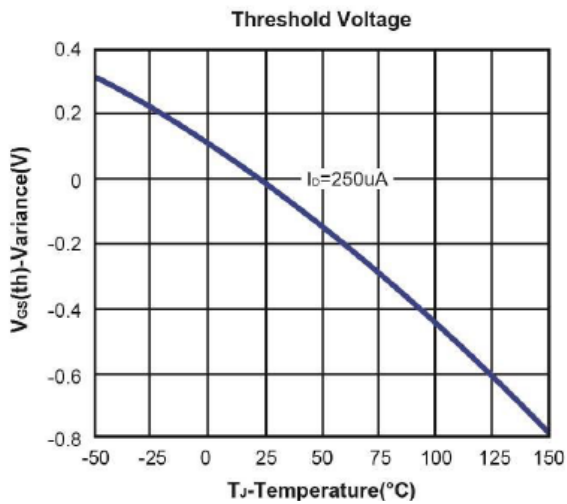
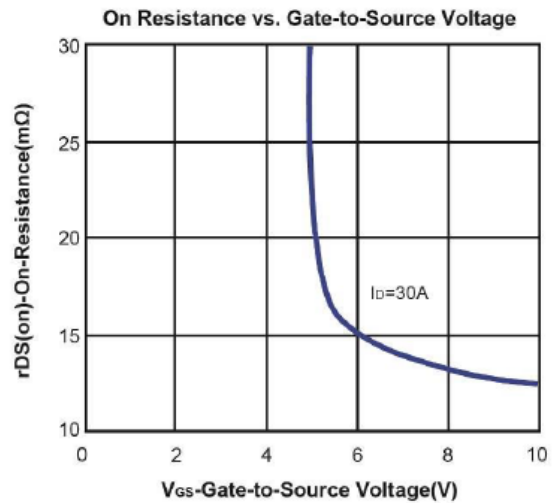
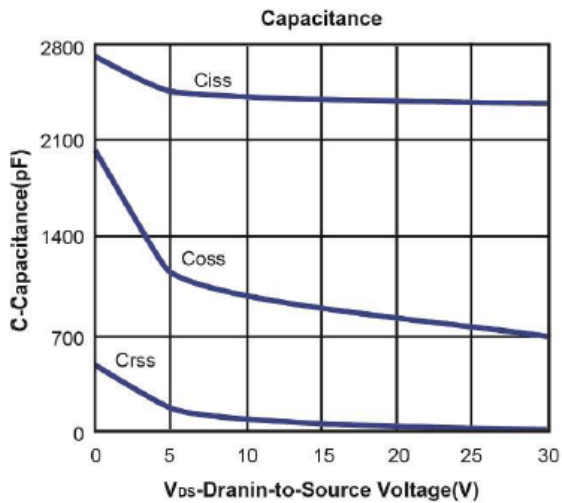
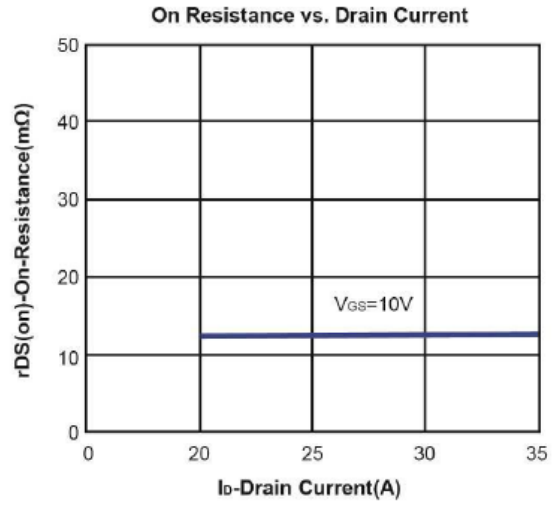
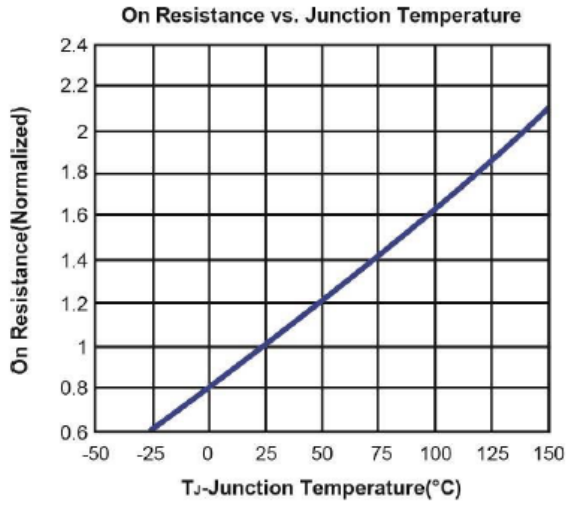
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$ $T_J = 25^\circ C$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J = 55^\circ C$			5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$		12.5	14	m $\Omega$
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$		0.6	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g(10V)$	$V_{DS}=50V, V_{GS}=10V$ $I_D=11.5A$		40		nC
Gate-Source Charge	$Q_{gs}$			9		
Gate-Drain Charge	$Q_{gd}$			6		
Input Capacitance	$C_{iss}$	$V_{DD}=30V, V_{GS}=0V$ $f=1MHz$		2342		pF
Output Capacitance	$C_{oss}$			702		
Reverse Transfer Capacitance	$C_{rss}$			38		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V,$ $I_D=30A, V_{GS}=10V$ $R_G=6\Omega$		8.4		nS
	$t_r$			30.3		
Turn-Off Time	$t_{d(off)}$			25.4		
	$t_f$			12.8		



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### TYPICAL CHARACTERISTICS

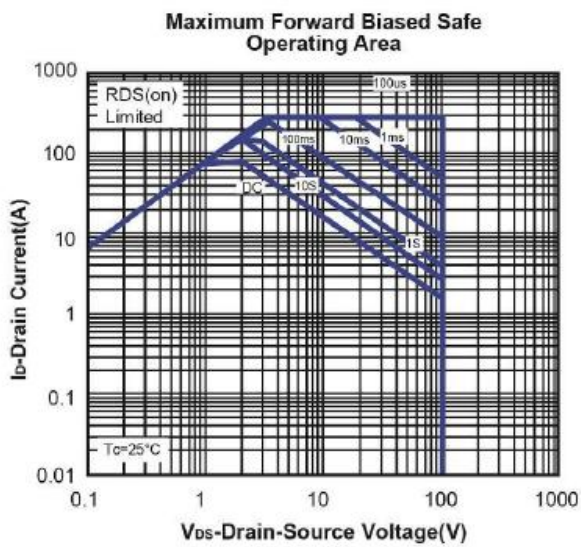
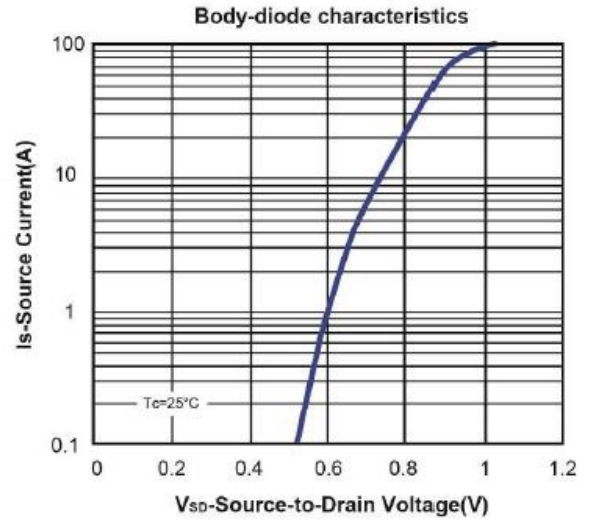
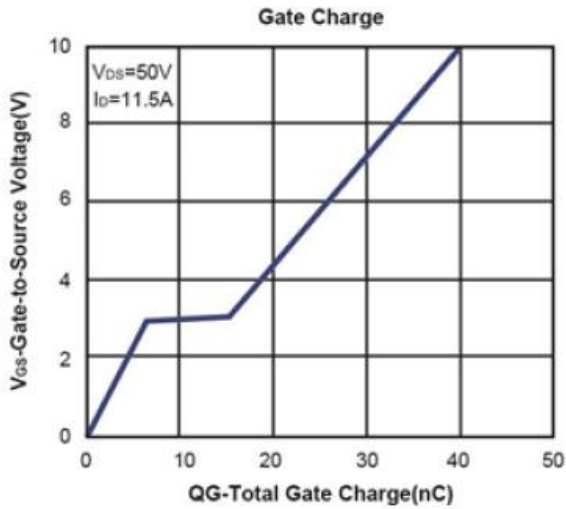




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### TYPICAL CHARACTERISTICS

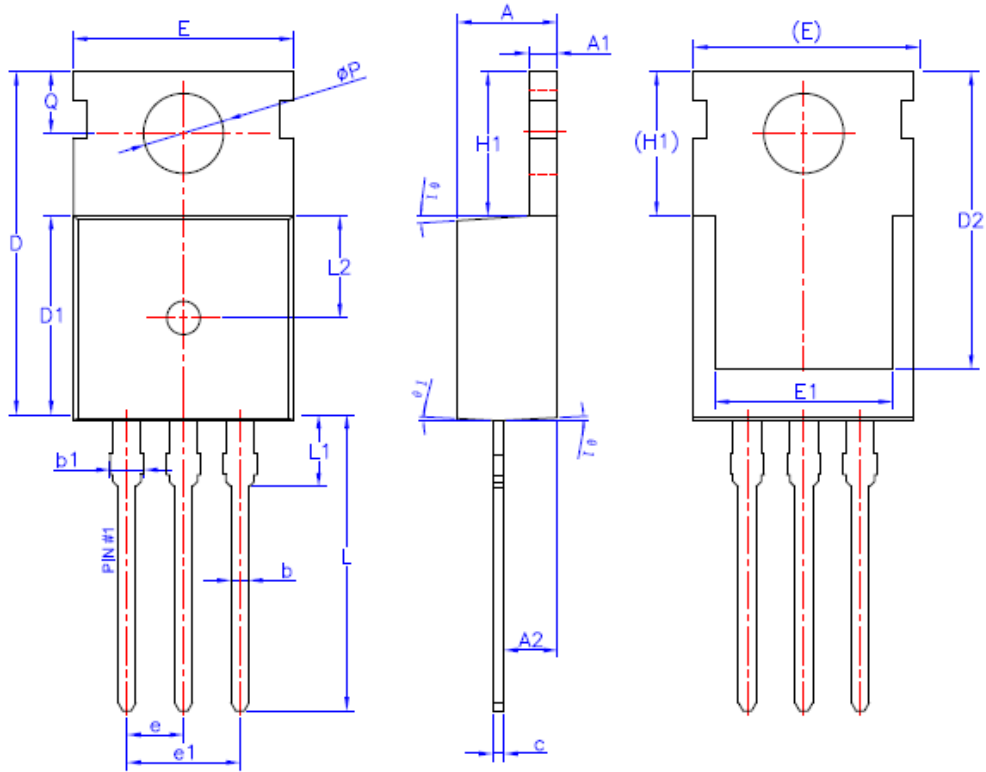




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## N-Channel Enhancement Mode MOSFET

### TO-220-3L PACKAGE OUTLINE



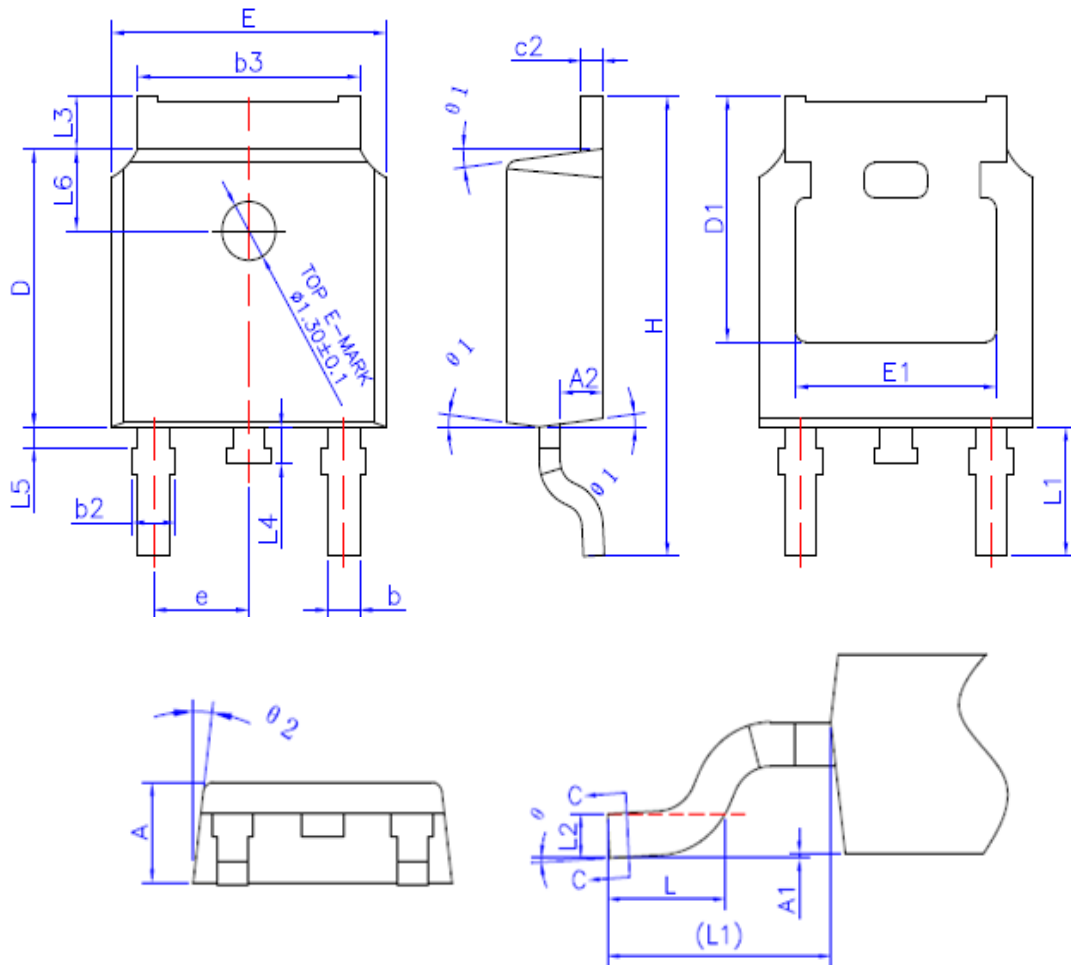
SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	—	2.87
$\theta 1$	1°	3°	5°



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## N-Channel Enhancement Mode MOSFET

### TO-252-2L PACKAGE OUTLINE



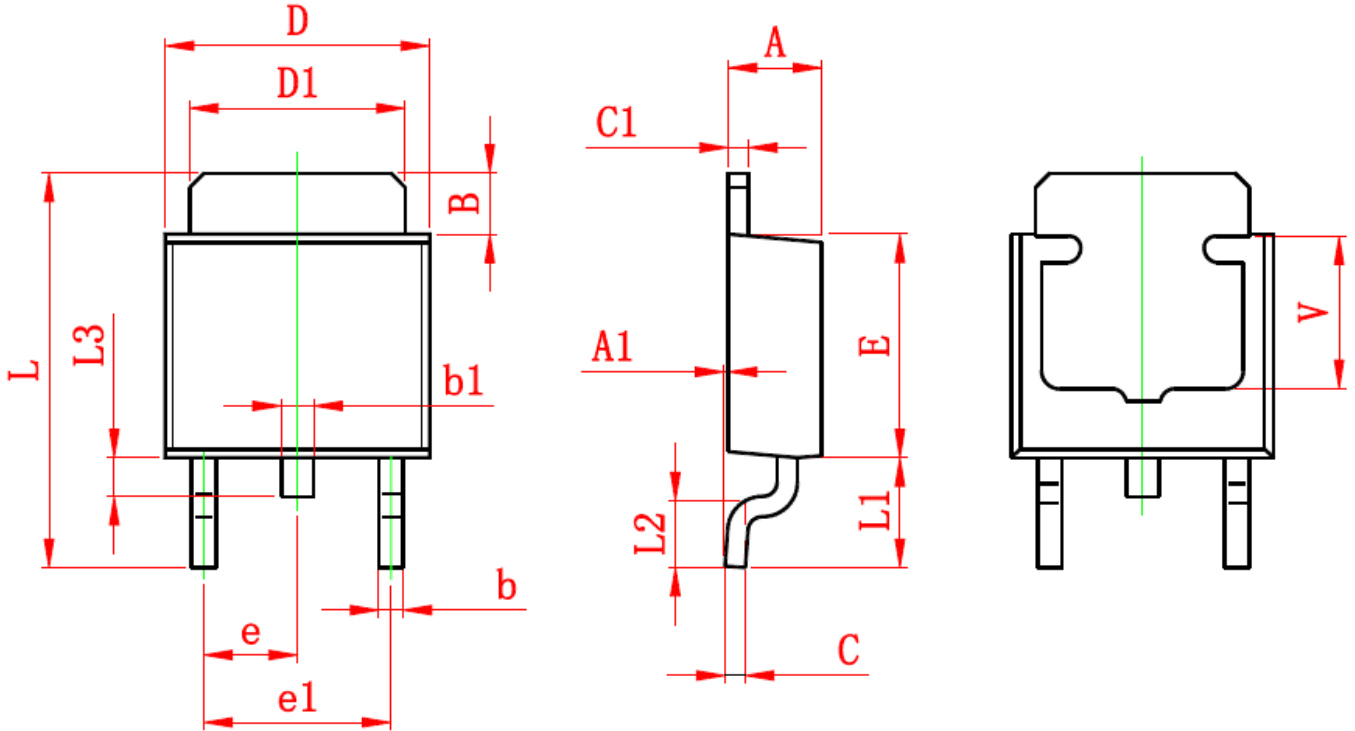
SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	--	0.15
A2	0.90	1.01	1.10
b	0.72	-	0.85
b2	0.72	--	0.90
b3	5.13	5.33	5.46
c	0.47	--	0.60
c2	0.47	--	0.60
D	6.00	6.10	6.20
D1	5.25	--	--
E	6.40	6.60	6.80
E1	4.70	--	--
e	2.3REF		
H	9.80	10.10	10.40
L	1.40	1.60	1.80
L1	2.90REF		
L2	0.508BSC		
L3	0.90	--	1.25
L4	0.60	0.80	1.00
L5	0.15	--	0.75
L6	1.80REF		
theta	0°	3°	8°
theta 1	5°	7°	9°
theta 2	5°	7°	9°



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### TO-252-2L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	





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