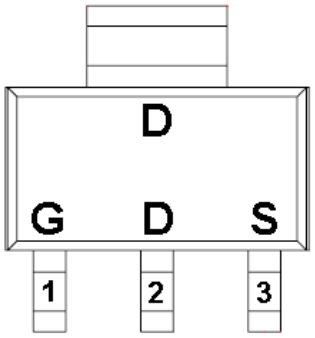
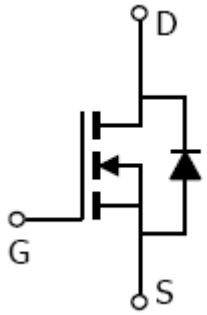
SPN8460
N-Channel Enhancement Mode MOSFET

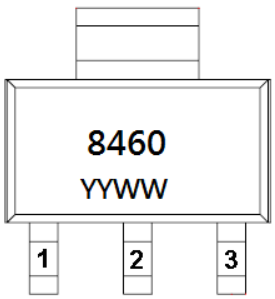
DESCRIPTION
The SPN8460 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a small outline surface mount package.

APPLICATIONS
- Power Tool
- DC/DC Converter
- Load Switch

FEATURES
- 60V/2.5A,$R_{DS(ON)}$=120mΩ@V_{GS}=10V
- 60V/2.0A,$R_{DS(ON)}$=130mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-223 package design

PIN CONFIGURATION(SOT-223)




PART MARKING


Y : Year Code
W : Week Code

SPN8460
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8460S22RGB	SOT-223	8460

※ SPN8460S22RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	4	A
	T_A=70℃		2.8	
Pulsed Drain Current		I_{DM}	25	A
Continuous Source Current(Diode Conduction)		I_S	2.5	A
Power Dissipation	T_A=25℃	P_D	3	W
	T_A=70℃		1.1	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	42	℃/W

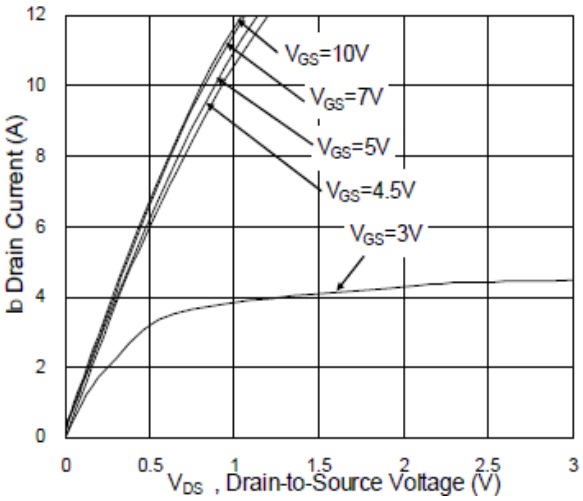
SPN8460
N-Channel Enhancement Mode MOSFET

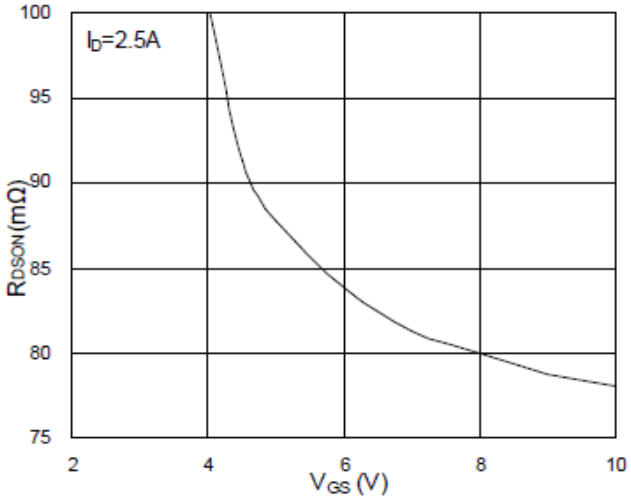
ELECTRICAL CHARACTERISTICS

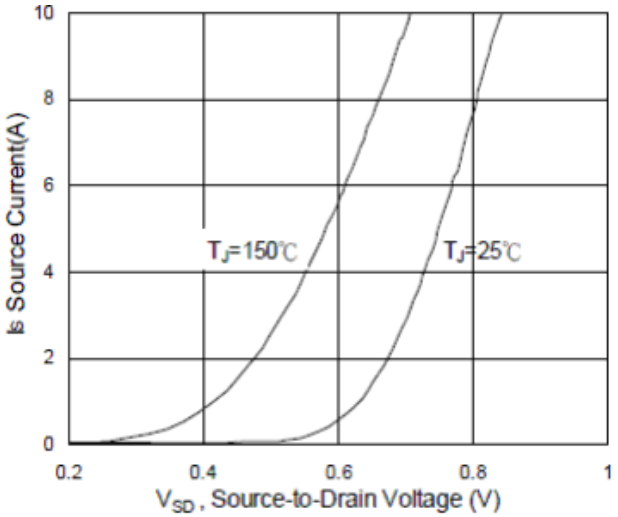
(T_A=25℃ Unless otherwise noted)

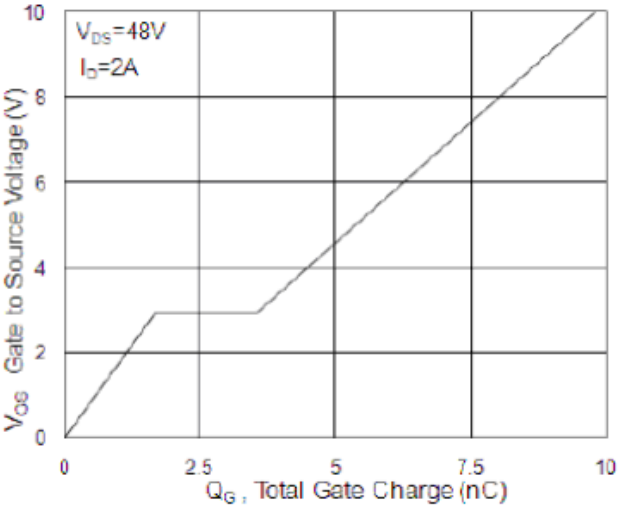
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.5		1.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V			1	uA
		V_{DS}=48V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≧10V,V_{GS}=4.5V	4			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V,I_D=2.5A			120	mΩ
		V_{GS} =4.5V,I_D=2A			130	
Forward Transconductance	gfs	V_{DS}=5V,I_D=2A		7		S
Diode Forward Voltage	V_{SD}	I_S=2.5A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=48V, V_{GS}=4.5V I_D=2A		5	7	nC
Gate-Source Charge	Q_{gs}			1.68	2.4	
Gate-Drain Charge	Q_{gd}			1.9	2.7	
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V f=1MHz		511		pF
Output Capacitance	C_{oss}			38		
Reverse Transfer Capacitance	C_{rss}			25		
Turn-On Time	$t_{d(on)}$	V_{DS}=30V, I_D=2.0A, V_{GS}=10V, R_G=3.3Ω		1.6	3.2	ns
	t_r			7.2	13	
Turn-Off Time	$t_{d(off)}$			25	50	
	t_f			14.5	29	

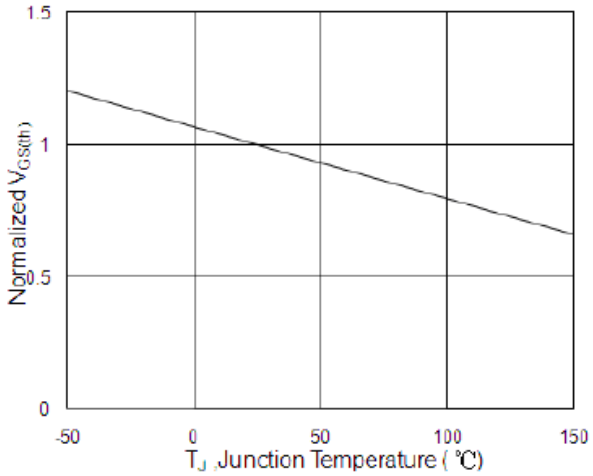
TYPICAL CHARACTERISTICS

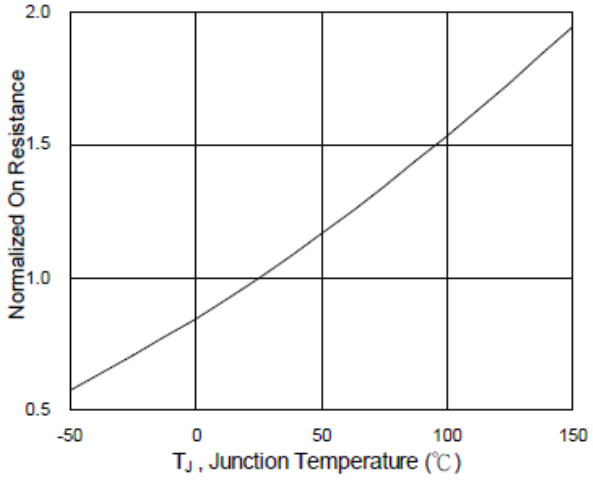




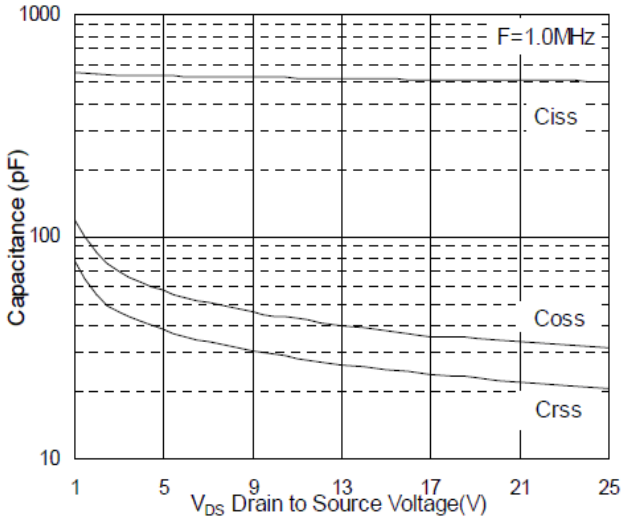


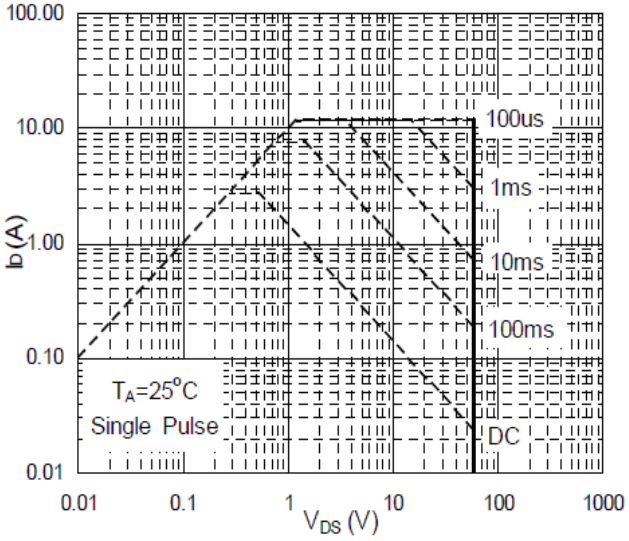


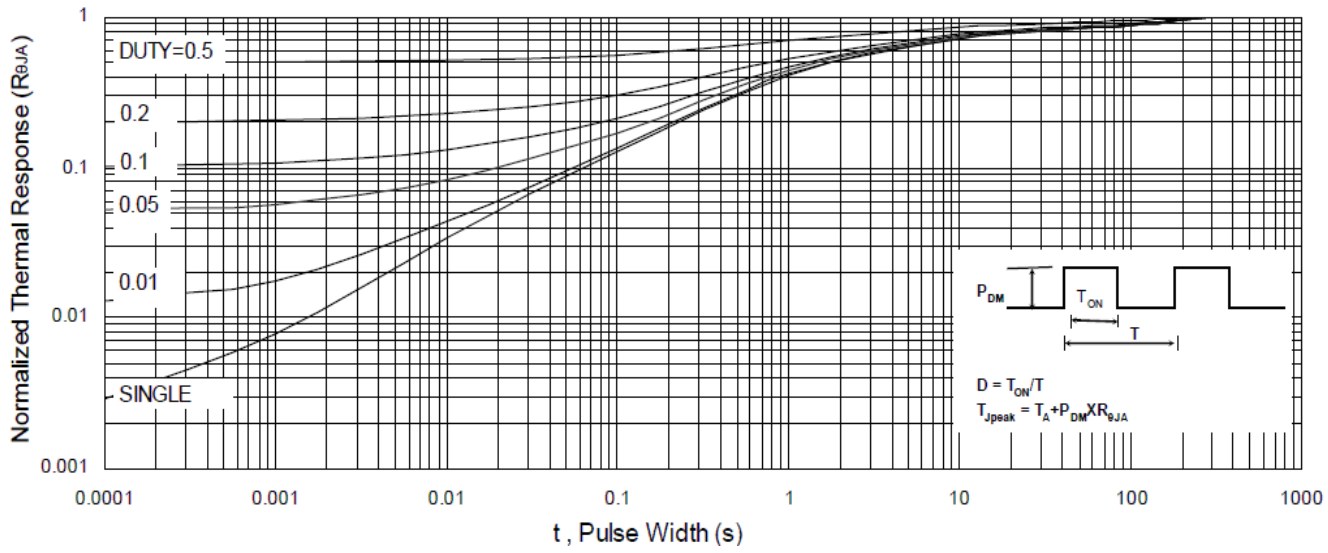


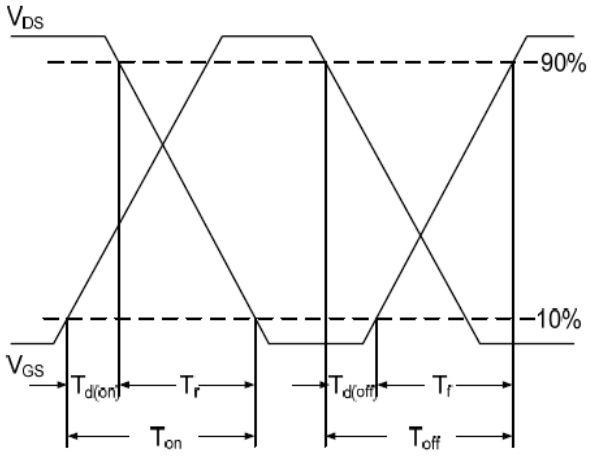


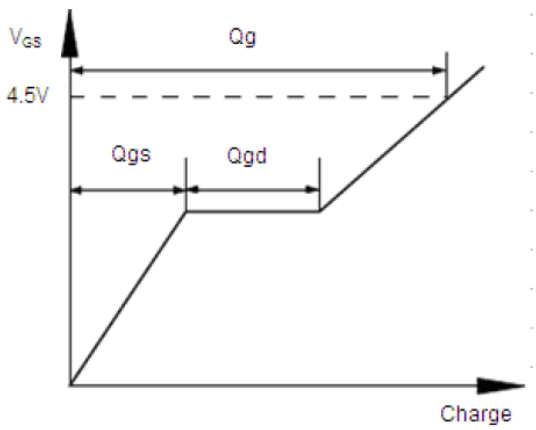
TYPICAL CHARACTERISTICS



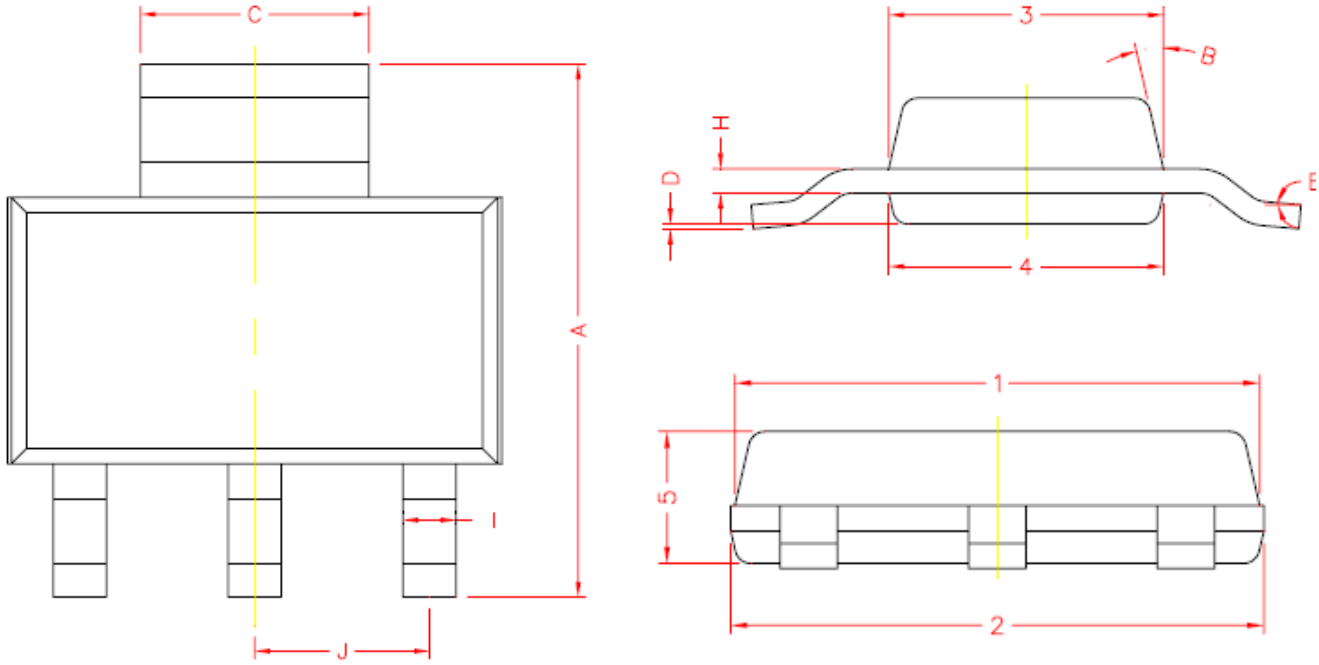








SOT-233 PACKAGE OUTLINE



REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	6.70	7.30
C	2.90	3.10
D	0.02	0.10
E	0°	10°
I	0.60	0.80
H	0.25	0.35
B	13° TYP.	
J	2.30 REF.	
1	6.30	6.70
2	6.30	6.70
3	3.30	3.70
4	3.30	3.70
5	1.40	1.80

7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan, 115, R.O.C
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
© http://www.syncpower.com