



SPN8636

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8636 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8636 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

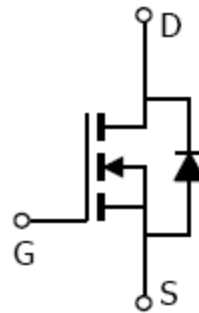
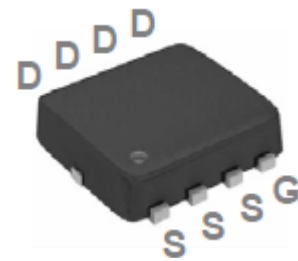
- ◆ 30V/80A, $R_{DS(ON)}=6.0m\Omega@V_{GS}=10V$
- ◆ 30V/80A, $R_{DS(ON)}=9.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3-8L package design

APPLICATIONS

- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

PPAK3x3-8L



PART MARKING





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PPAK3x3-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8636DN8RGB	PPAK3x3-8L	SPN8636

※ SPN8636DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	I _D	T _C =25°C	80
		T _C =100°C	57
Pulsed Drain Current	I _{DM}	160	A
Avalanche Current	I _{AS}	50	A
Single Pulse Avalanche Energy	E _{AS}	180	mJ
Power Dissipation	P _D	83	W
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	1.5	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$			80	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		4.7	6.0	mΩ
		$V_{GS}=4.5V, I_D=10A$		6.5	9.0	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=30A$		22		S
Diode Forward Voltage	V_{SD}	$I_S=1A, V_{GS}=0V$			1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V$ $I_D=15A$		20	18	nC
Gate-Source Charge	Q_{gs}			7.6		
Gate-Drain Charge	Q_{gd}			7.2		
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1MHz$		2300		pF
Output Capacitance	C_{oss}			265		
Reverse Transfer Capacitance	C_{rss}			210		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V,$ $I_D=15A, V_{GEN}=10V$ $R_G=3.3\Omega$		7.8	15	nS
	t_r			15	12	
Turn-Off Time	$t_{d(off)}$			37	30	
	t_f			10.6	15	



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TYPICAL CHARACTERISTICS

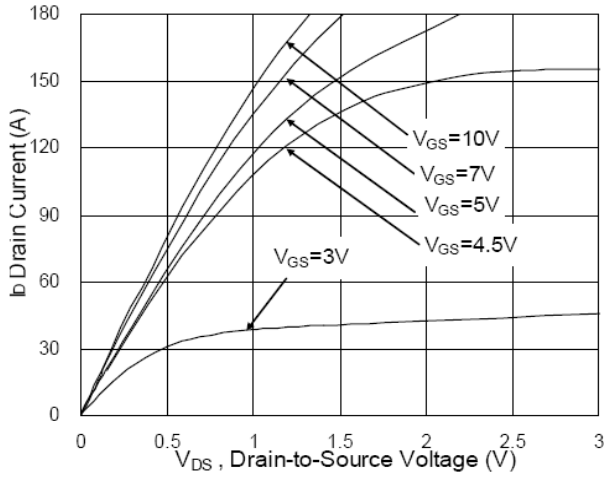


Fig. 1 Typical Output Characteristics

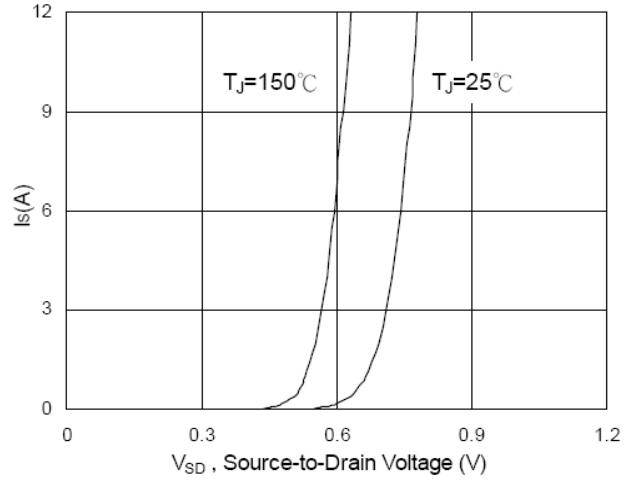


Fig. 2 Transfer Characteristics

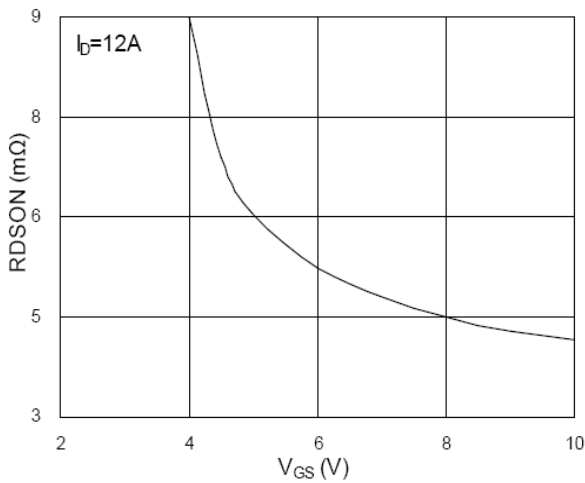


Fig. 3 On-Resistance vs Gate voltage

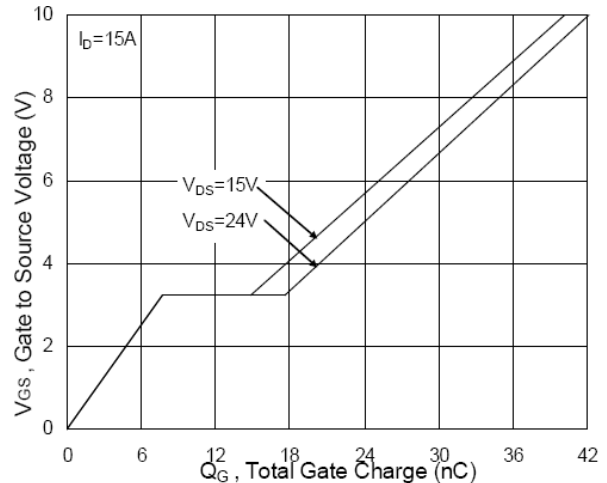


Fig. 4 Gate Charge Characteristics

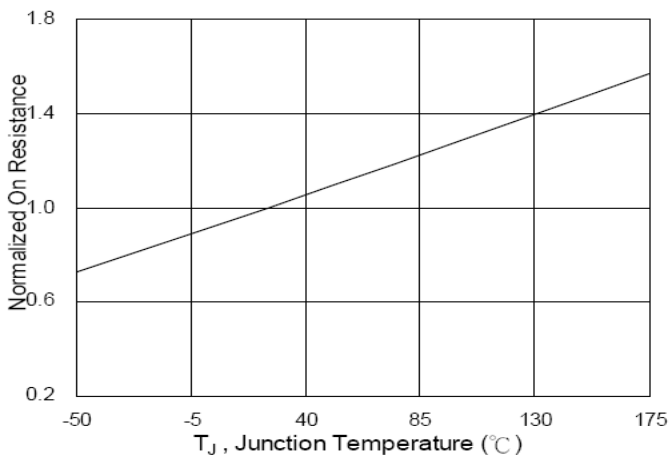


Fig. 5 On-Resistance vs Junction Temp

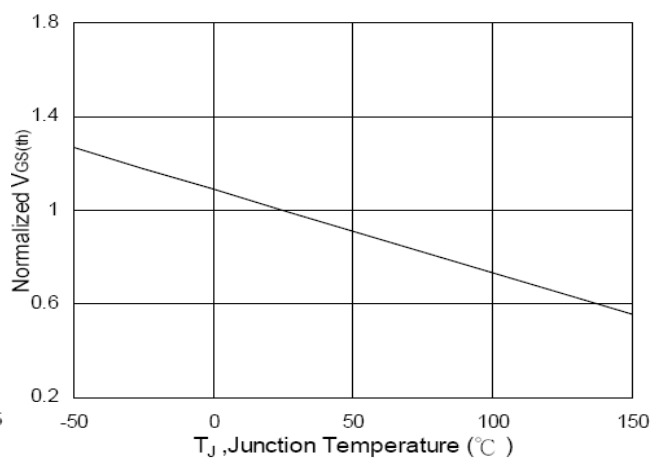


Fig. 6 V_{GS} vs Junction Temperature



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TYPICAL CHARACTERISTICS

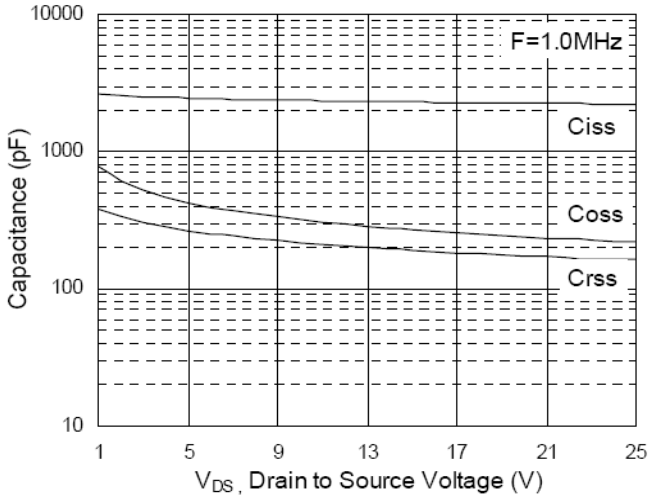


Fig. 7 Typical Capacitance Characteristics

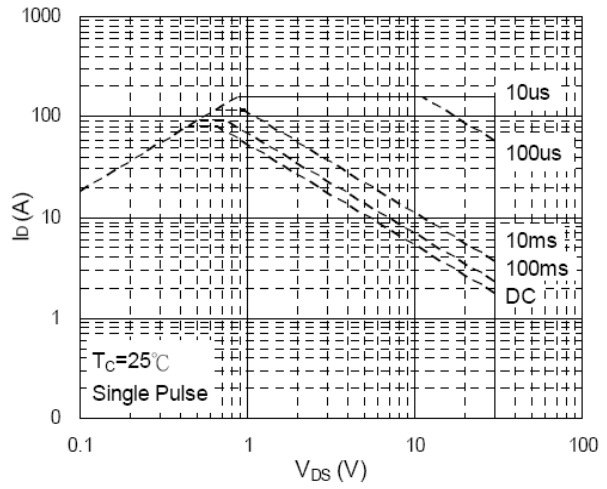


Fig. 8 Maximum Safe Operation Area

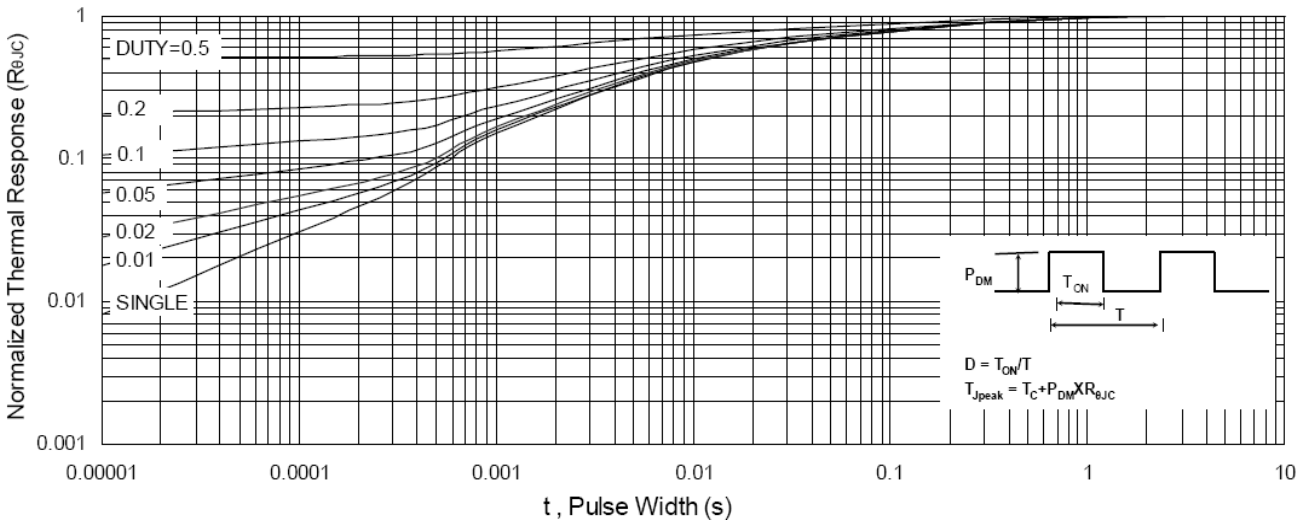


Fig. 9 Effective Transient Thermal Impedance

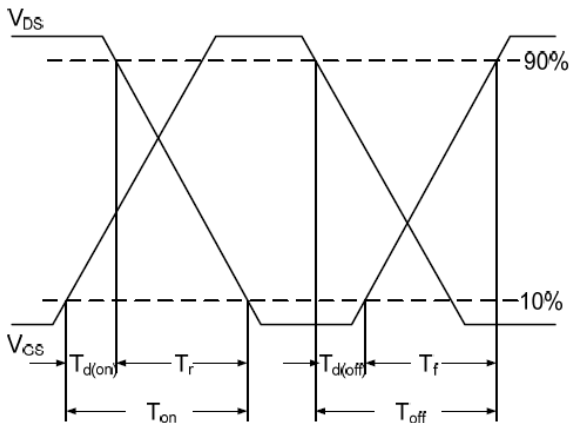


Fig. 10 Switching Time Waveform

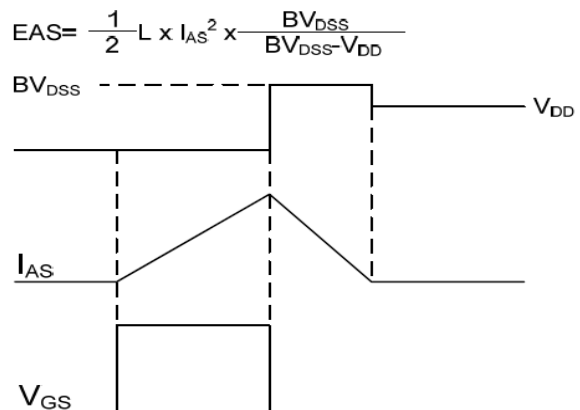


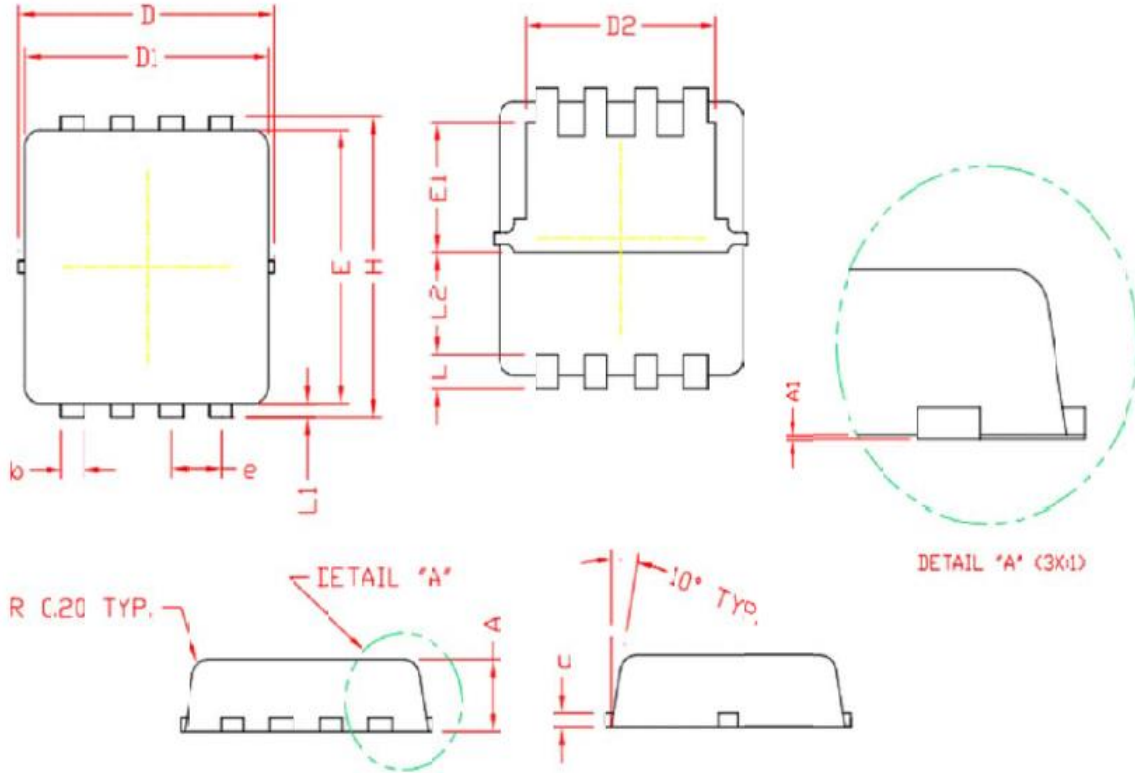
Fig. 11 Unclamped Inductive Waveform



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PPAK3x3-8L PACKAGE OUTLINE



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.80	0.90
A1	0.00	0.03	0.05
b	0.24	0.30	0.35
c	0.10	0.15	0.20
D	3.25	3.32	3.40
D1	3.05	3.15	3.25
D2	2.40	2.50	2.60
E	3.00	3.10	3.20
E1	1.35	1.45	1.55
e	0.65 BSC		
H	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.10	0.15	0.20
L2	1.13REF		



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