



SPN8834

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8834 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPN8834 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

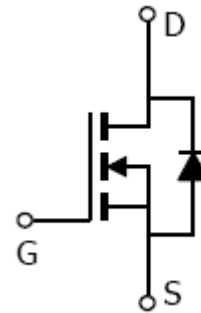
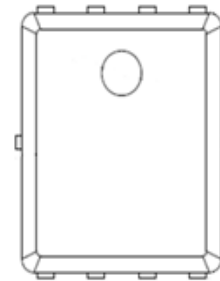
- ◆ 30V/96A, $R_{DS(ON)}=4.2m\Omega@V_{GS}=10V$
- ◆ 30V/96A, $R_{DS(ON)}=6.0m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

APPLICATIONS

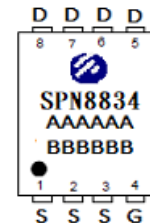
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch
- POL Applications

PIN CONFIGURATION

PPAK5x6-8L



PART MARKING



A : Lot Code
 B : Date Code
 (YY/MM/DD)



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PPAK5x6-8L PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8834DN8RGB	PPAK5x6-8L	SPN8834

※ SPN8834DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	I _D	T _C =25°C	96
		T _C =100°C	68
Pulsed Drain Current	I _{DM}	192	A
Avalanche Current	I _{AS}	53.8	A
Single Pulse Avalanche Energy	E _{AS}	317	mJ
Power Dissipation	P _D	83	W
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	1.5	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ C$			1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=125^\circ C$			10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=30A$		3.8	4.2	mΩ
		$V_{GS}=4.5V, I_D=15A$		5.2	6	
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=6A$		12		S
Diode Forward Voltage	V_{SD}	$I_F=1A, V_{GS}=0V$			1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=12A$		24	34	nC
Gate-Source Charge	Q_{gs}			4.2	6	
Gate-Drain Charge	Q_{gd}			13	18	
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $F=1MHz$		2200	3190	pF
Output Capacitance	C_{oss}			280	405	
Reverse Transfer Capacitance	C_{rss}			177	255	
Turn-On Time	$t_{d(on)}$	$(V_{DD}=15V, I_D=15A,$ $V_{GEN}=10V, R_G=3.3\Omega)$		12.6	24	ns
	t_r			19.5	37	
Turn-Off Time	$t_{d(off)}$			42.8	81	
	t_f			13.2	25	



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TYPICAL CHARACTERISTICS

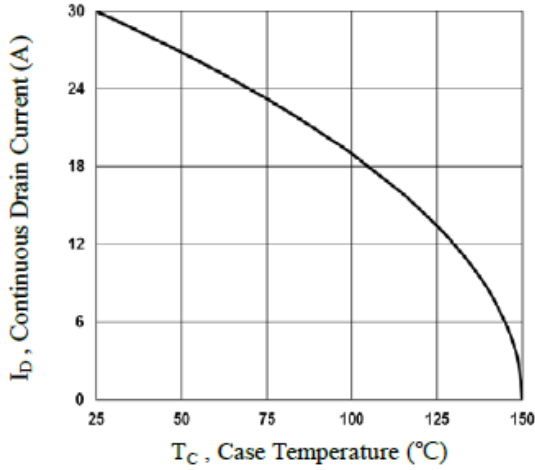


Fig.1 Continuous Drain Current vs. T_C

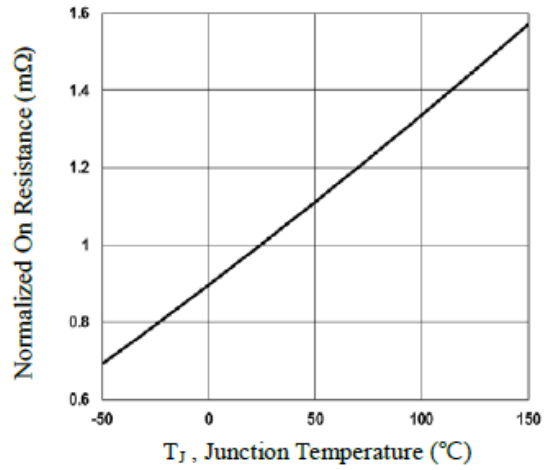


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

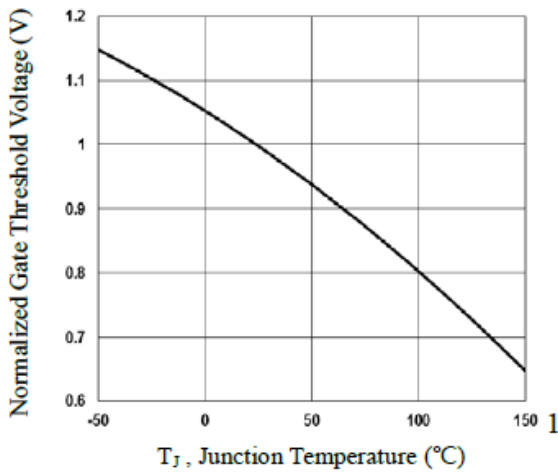


Fig.3 Normalized V_{th} vs. T_J

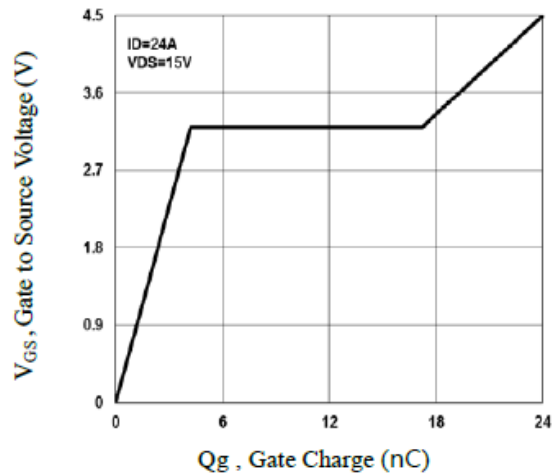


Fig.4 Gate Charge Waveform

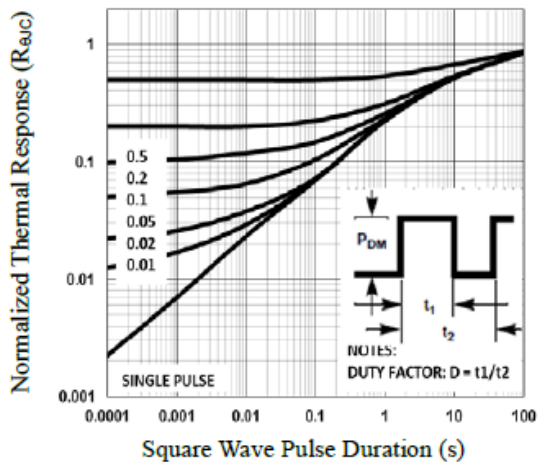


Fig.5 Normalized Transient Impedance

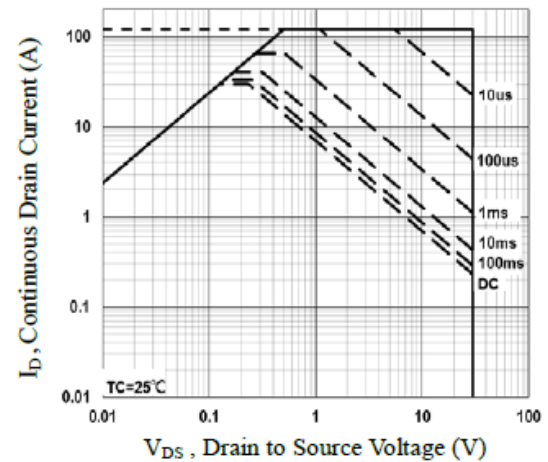


Fig.6 Maximum Safe Operation Area



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TYPICAL CHARACTERISTICS

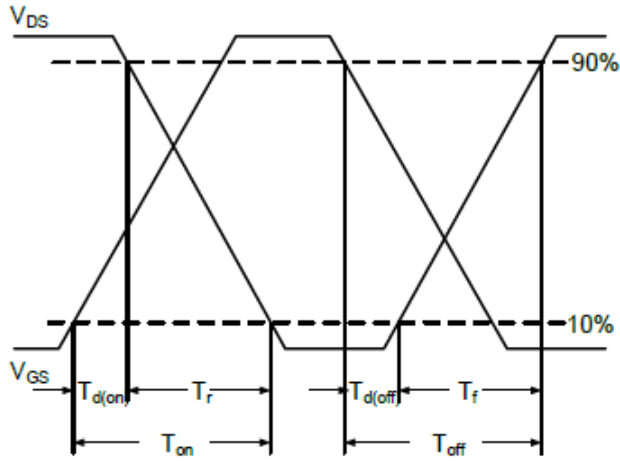


Fig.7 Switching Time Waveform

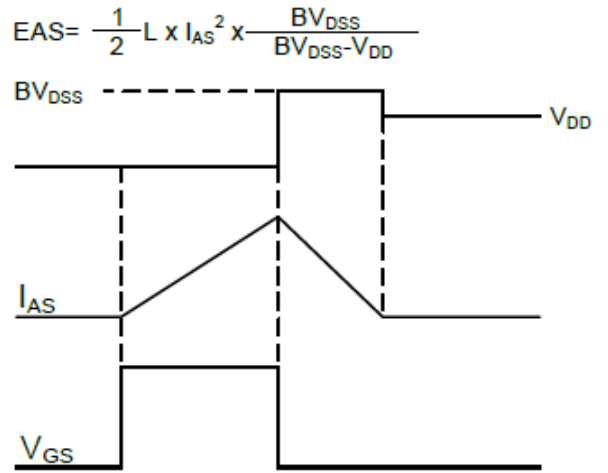
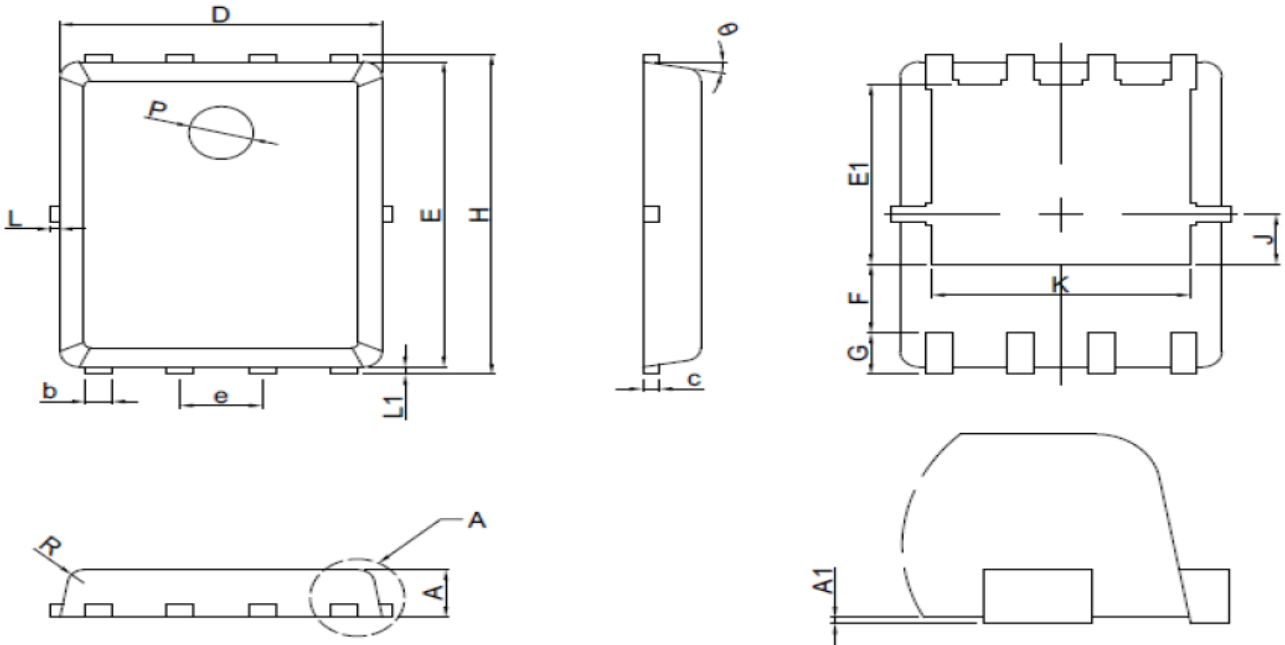


Fig.8 EAS Waveform



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PPAK5x6-8L PACKAGE OUTLINE



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.8	0.95	1.1
A1	0.00	0.03	0.05
b	0.33	0.41	0.51
c	0.254 REF		
D	4.80	4.95	5.10
F	1.40 REF		
E	5.70	5.80	5.90
e	1.27 BSC		
H	5.90	6.05	6.20
L1	0.06	0.13	0.20
G	0.60 REF		
J	0.95 BSC		
K	4.00 REF		
L	---	----	0.20
P	1.00 REF		
E1	3.40REF		
E2	0.95 REF		
θ	6°	10°	14°
R	0.25REF		



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