



SPN8852

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8852 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

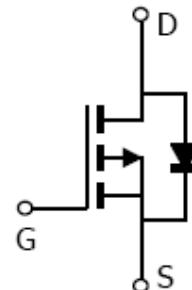
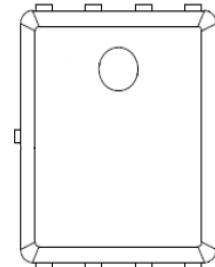
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

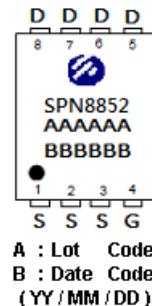
FEATURES

- ◆ 150V/4.1A,R_{DS(ON)}=88mΩ@V_{GS}=10V
- ◆ 150V/2A,R_{DS(ON)}=100mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low R_{DS (ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

PIN CONFIGURATION(PPAK5x6-8L)



PART MARKING





SPN8852

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8852DN8RGB	PPAK5x6-8L	SPN8852

※ SPN4852S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	150	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	I _D	4.1	A
Pulsed Drain Current	I _{DM}	20	A
Avalanche Energy, Single Pulse (L=0.1mH , T _c =25°C)	E _{AS}	40	mJ
Power Dissipation	T _c =25°C	P _D	W
	TA=25°C		
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	R _{θJC}	25	°C/W
Thermal Resistance-Junction to Ambient (steady state)	R _{θJA}	50	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	150			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	1.2		2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =120V, V _{GS} =0V T _J =25°C			1	uA
		V _{DS} =120V, V _{GS} =0V T _J =100°C			100	
Drain-Source On-Resistance	R _{D(on)}	V _{GS} = 10V, ID=4.1A			88	mΩ
		V _{GS} =4.5V, ID=2A			100	
Forward Transconductance	g _{fs}	V _{DS} =5V, ID=10A		33		S
Diode Forward Voltage	V _{SD}	I _s =1A, V _{GS} =0V			1.0	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =75V, V _{GS} =4.5V, ID=10A		25.1		nC
Gate-Source Charge	Q _{gs}			8.8		
Gate-Drain Charge	Q _{gd}			12.6		
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1MHz		2280		pF
Output Capacitance	C _{oss}			110		
Reverse Transfer Capacitance	C _{rss}			83		
Turn-On Time	t _{d(on)}	V _{DD} =75V, ID=10A, V _{GS} =10V R _G =3.3Ω		13		nS
	t _r			8.2		
Turn-Off Time	t _{d(off)}			25		
	t _f			11		



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TYPICAL CHARACTERISTICS

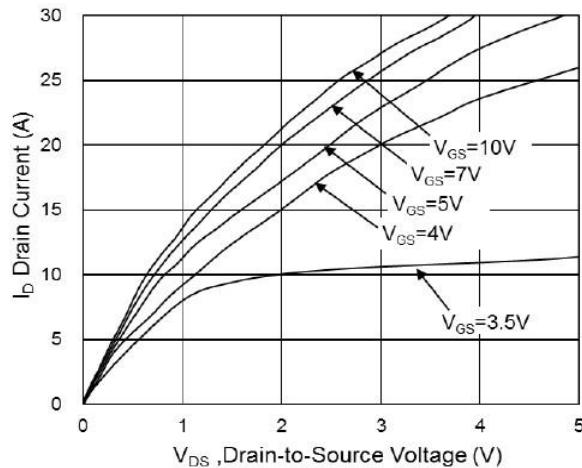


Fig.1 Typical Output Characteristics

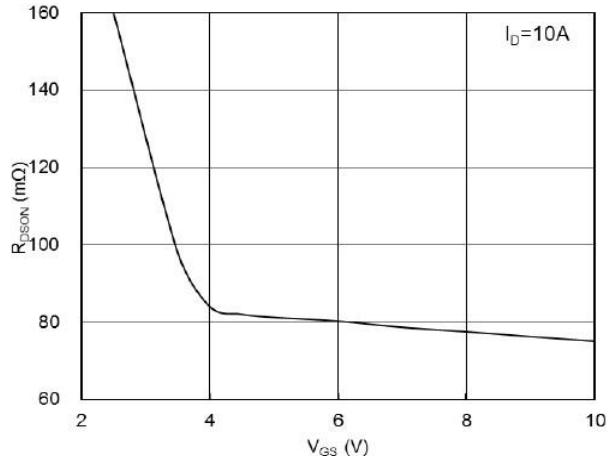


Fig.2 On-Resistance vs. Gate-Source Voltage

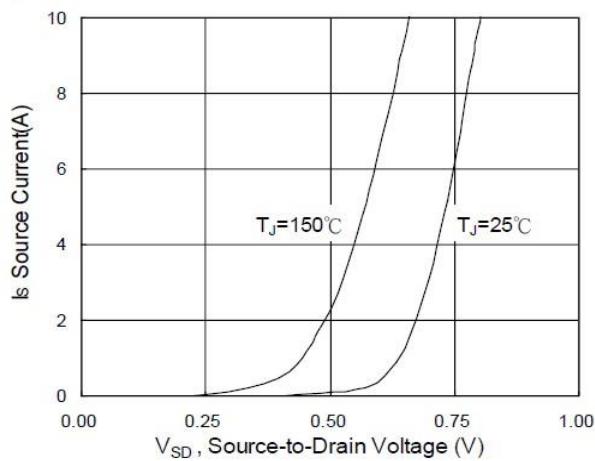


Fig.3 Forward Characteristics of Reverse

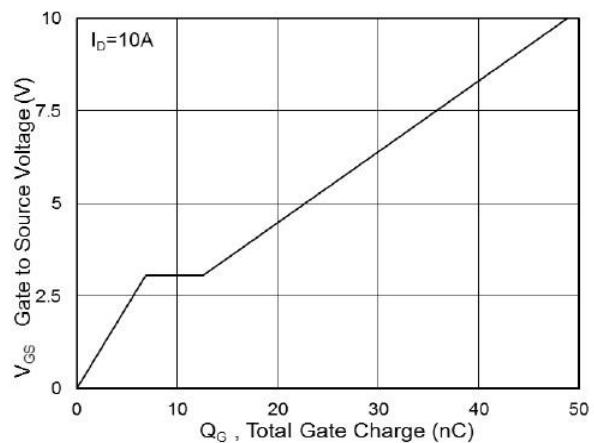


Fig.4 Gate-Charge Characteristics

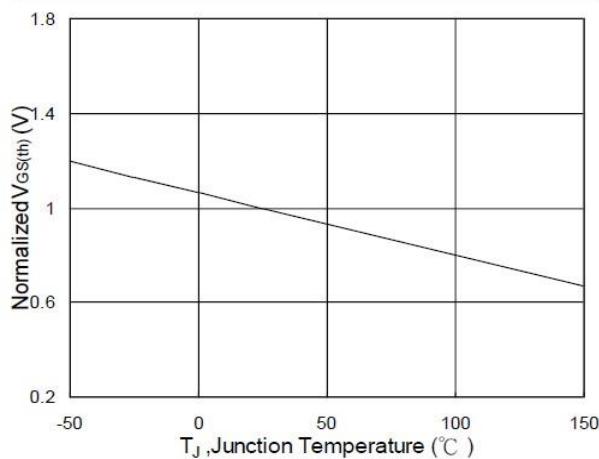


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

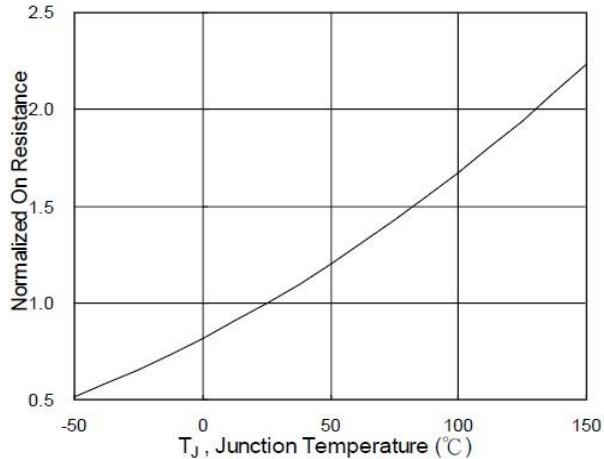


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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TYPICAL CHARACTERISTICS

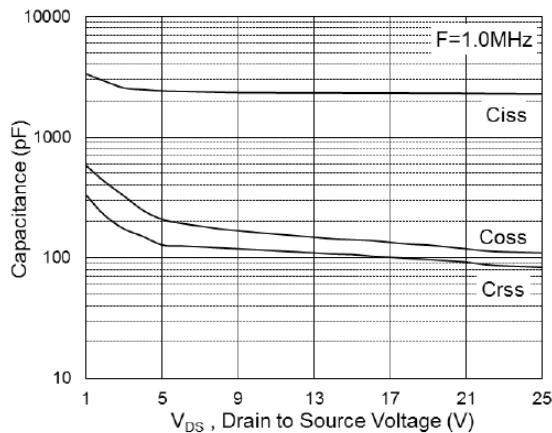


Fig.7 Capacitance

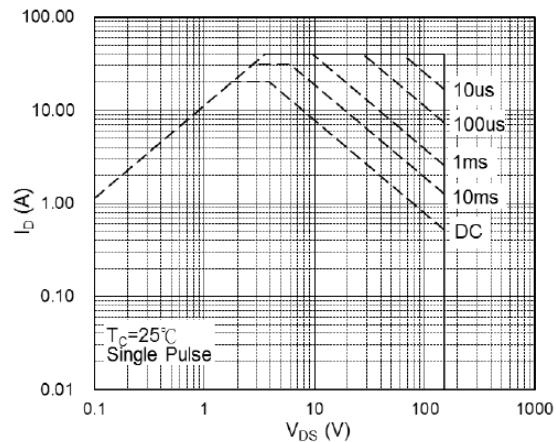


Fig.8 Safe Operating Area

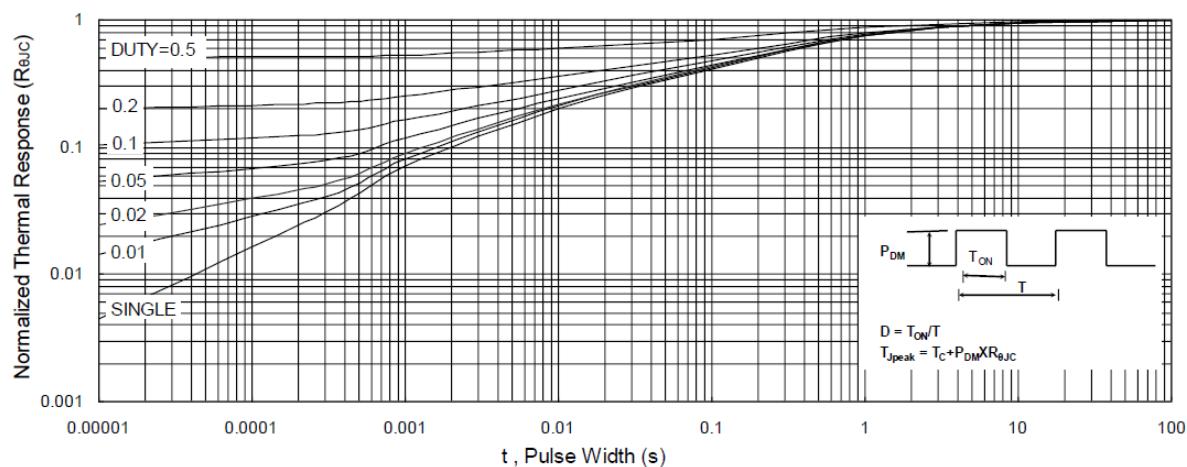


Fig.9 Normalized Maximum Transient Thermal Impedance

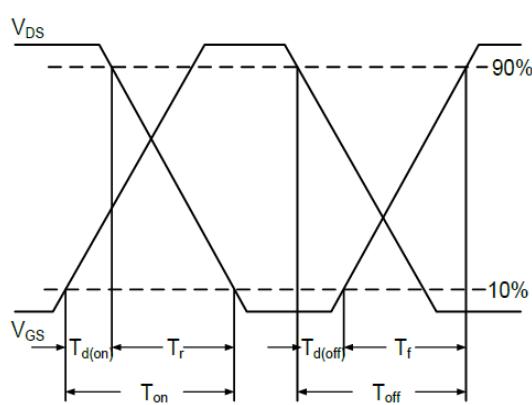


Fig.10 Switching Time Waveform

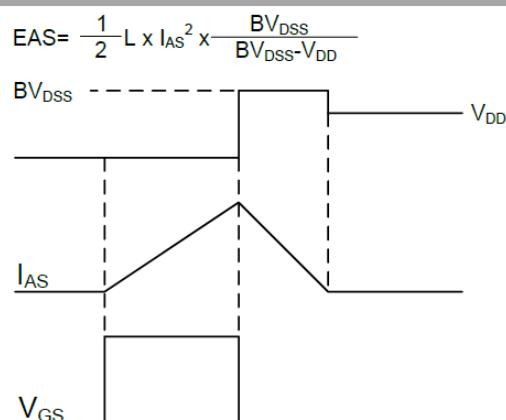


Fig.11 Unclamped Inductive Switching Waveform

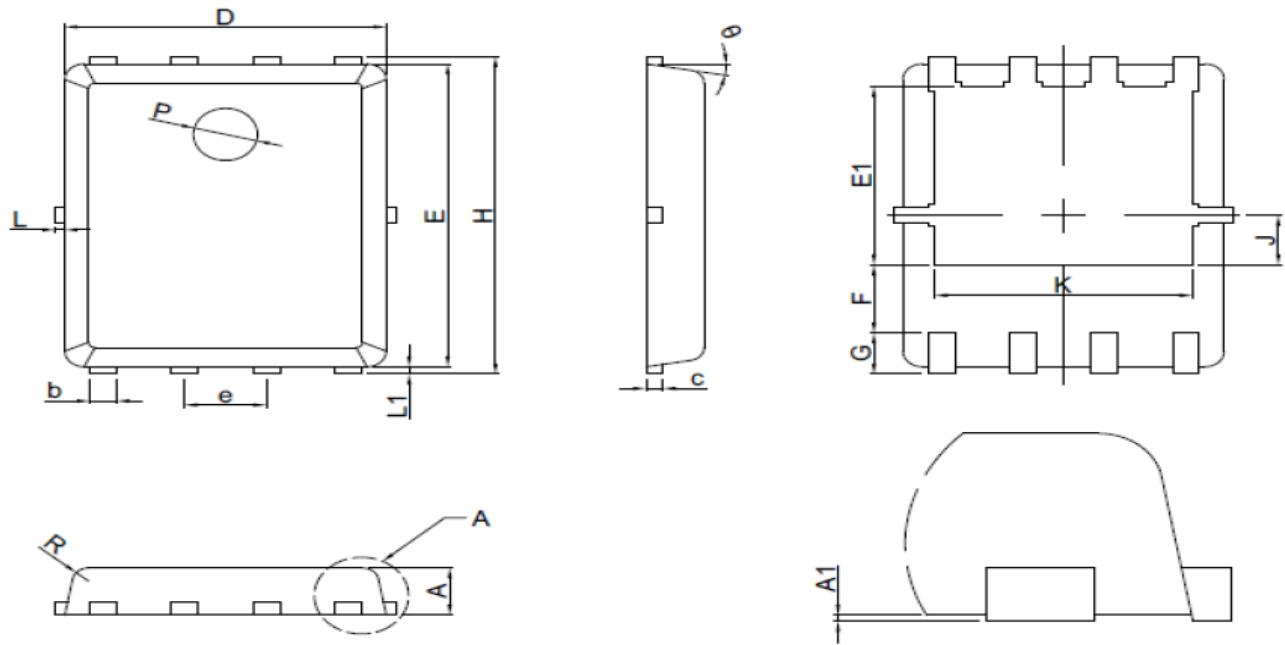
SOP- 8



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PPAK5x6-8L PACKAGE OUTLINE



SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.8	0.95	1.1
A1	0.00	0.03	0.05
b	0.33	0.41	0.51
c	0.254 REF		
D	4.80	4.95	5.10
F	1.40 REF		
E	5.70	5.80	5.90
e	1.27 BSC		
H	5.90	6.05	6.20
L1	0.06	0.13	0.20
G	0.60 REF		
J	0.95 BSC		
K	4.00 REF		
L	---	----	0.20
P	1.00 REF		
E1	3.40REF		
E2	0.95 REF		
θ	6°	10°	14°
R	0.25REF		



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