SPP2323
Dual P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2323 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

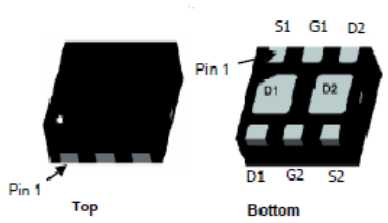
APPLICATIONS

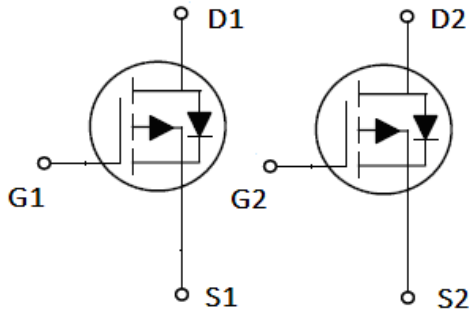
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

- -20V/-3.3A,$R_{DS(ON)}$=65mΩ@ V_{GS}=-4.5V
  -20V/-2.8A,$R_{DS(ON)}$=85mΩ@V_{GS}=-2.5V
  -20V/-2.3A,$R_{DS(ON)}$=130mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TDFN2x2-6L package design

PIN CONFIGURATION(TDFN2x2-6L)





PART MARKING

Y : Year Code
W: Week Code

SPP2323

Dual P-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	D2	Drain 2
4	S2	Source 2
5	G2	Gate 2
6	D1	Drain1
Exposed Backside Metal	D1/D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2323TDN6RGB	TDFN2x2-6L	2323YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP2323TDN6RGB : Tape Reel ; Pb – Free ; Halogen -Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate –Source Voltage		V_{GSS}	±10	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-4.0	A
	T_A=100℃		-2.8	
Pulsed Drain Current		I_{DM}	-16	A
Continuous Source Current(Diode Conduction)		I_S	-1.6	A
Power Dissipation	T_A=25℃	P_D	1.9	W
	T_A=70℃		1.2	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient	T ≤ 5sec	$R_{\theta JA}$	65	℃/W
	Steady State		95	

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.3		-1.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±10V			-10	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V			-1	uA
		V_{DS}=-16V,V_{GS}=0V T_J=125℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≤ -4.5V,V_{GS} =-5V	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-3.3A		45	65	mΩ
		V_{GS}=-2.5V,I_D=-2.8A		60	85	
		V_{GS}=-1.8V,I_D=-2.3A		90	130	
		V_{GS}=-1.5V,I_D=-1A		100	140	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-1A		2.2		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V			-1	V
Dynamic						
Input Capacitance	C_{iss}	V_{DS}=--10V, V_{GS}=-0V ,F=1MHz		515	745	pF
Output Capacitance	C_{oss}			55	80	
Reverse Transfer Capacitance	C_{rss}			20	30	
Total Gate Charge	Q_g	V_{DS}=--10V, V_{GS}=-4.5V ,I_D=-3A		6.4		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-On Time	$t_{d(on)}$	V_{DD}=-10V, I_D=-1A V_{GEN}=-4.5V ,R_G=25Ω		5		nS
	t_r			17.4		
Turn-Off Time	$t_{d(off)}$			40.7		
	t_f			11.4		

TYPICAL CHARACTERISTICS

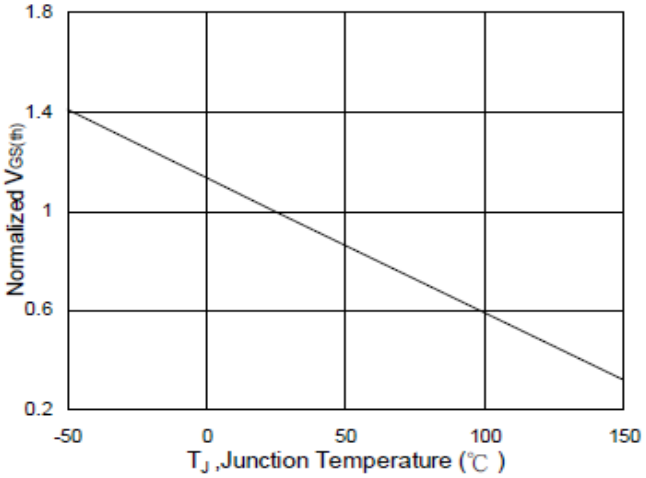


Fig. 1 Normalized Vgs(th) vs. Temp

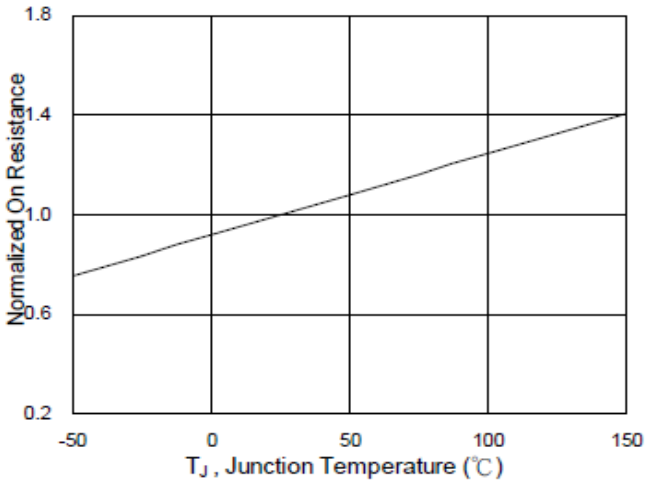


Fig. 2 Normalized On-Resistance vs. Temp

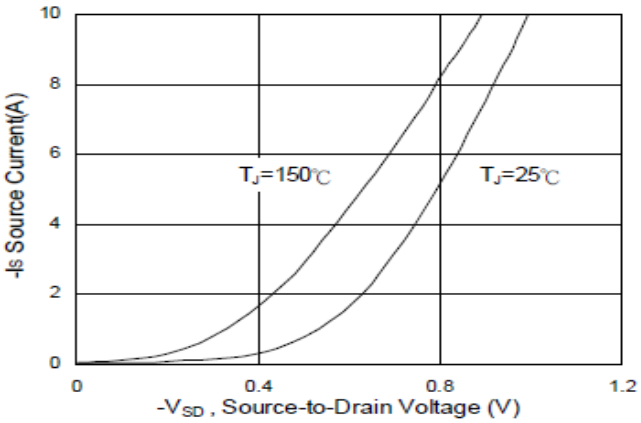


Fig. 3 Output Characteristics

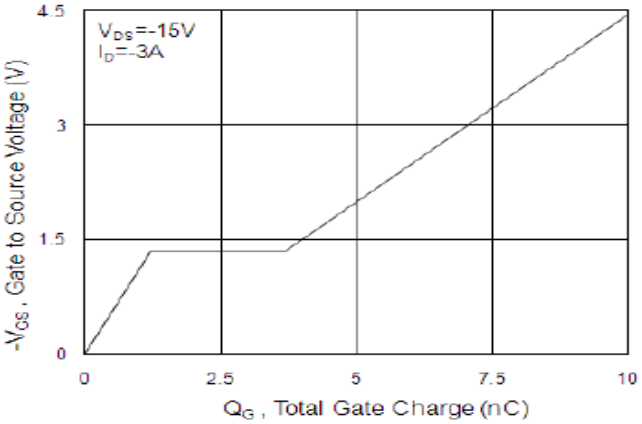


Fig. 4 Gate Charge Characteristics

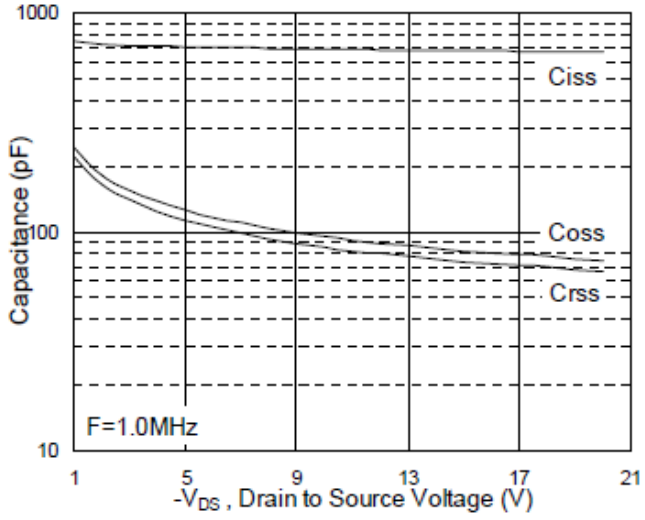


Fig 5 Capacitance vs. Drain Voltage

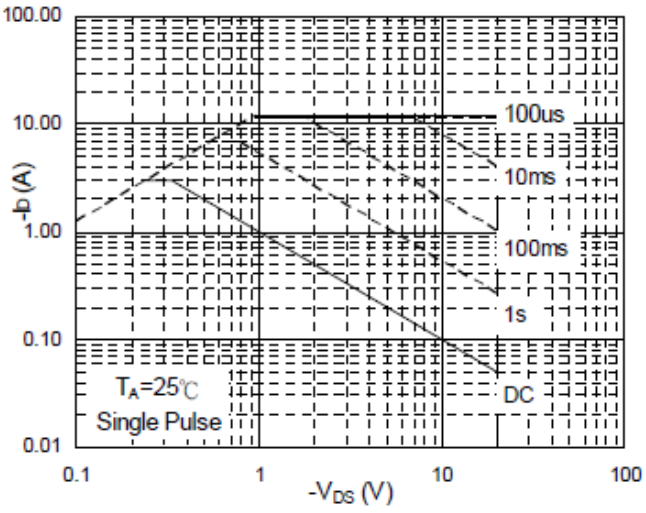
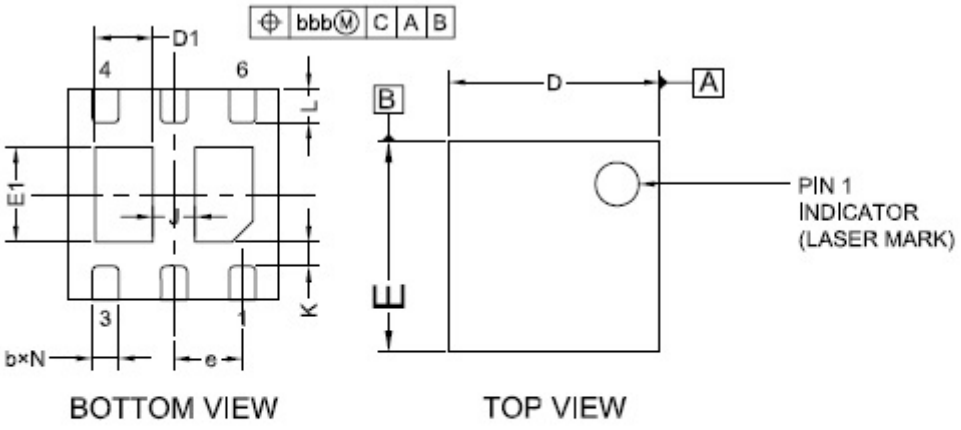
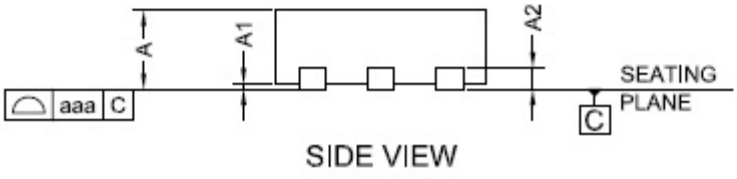


Fig. 6 Safe Operation Area

TDFN2x2-6L PACKAGE OUTLINE





COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D1	0.50	0.55	0.60
E	1.95	2.00	2.05
E1	0.85	0.90	0.95
e		0.65BSC	
L	0.27	0.32	0.37
J		0.40BSC	
K		0.20MIN	
N		6	
aaa		0.08	
bbb		0.10	

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