



# SPP2325

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP2325 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

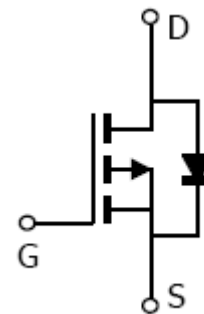
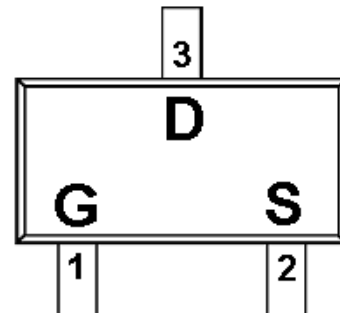
### FEATURES

- ◆ -100V/-3A, $R_{DS(ON)}=270m\Omega@V_{GS}=-10V$
- ◆ -100V/-1.5A, $R_{DS(ON)}=330m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

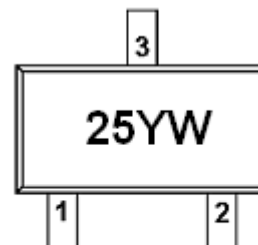
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(SOT-23)



### PART MARKING



Y : Year Code  
W : Week Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2325S23RGB	SOT-23	S25YW

※ Week Code : A ~ Z( 1 ~ 26 ) ; a ~ z( 27 ~ 52 )

※ SPP2325S23RGB : Tape Reel ; Pb – Free; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-3.0	A
		TA=70°C	-2.0	
Pulsed Drain Current	I <sub>DM</sub>	-4.5	A	
Power Dissipation	P <sub>D</sub>	TA=25°C	1.15	W
		TA=70°C	0.8	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	100	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-80V, V_{GS}=0V$ $T_J=25^\circ C$			-10	uA
		$V_{DS}=-80V, V_{GS}=0V$ $T_J=55^\circ C$			-100	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=V_{GS}=0V$			-3.0	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-1A$		225	270	mΩ
		$V_{GS}=-4.5V, I_D=-0.5A$		255	330	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-1A$		2.9		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1A, V_{GS}=0V$			-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-50V, V_{GS}=-10V$ $I_D=-1A$		9.3		nC
Gate-Source Charge	$Q_{gs}$			1.75		
Gate-Drain Charge	$Q_{gd}$			1.25		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		553		pF
Output Capacitance	$C_{oss}$			29		
Reverse Transfer Capacitance	$C_{rss}$			20		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-50V, I_D=-0.5A,$ $V_{GEN}=-10V, R_G=3.3\Omega$		2		ns
	$t_r$			18.4		
Turn-Off Time	$t_{d(off)}$			19.6		
	$t_f$			19.5		



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## TYPICAL CHARACTERISTICS

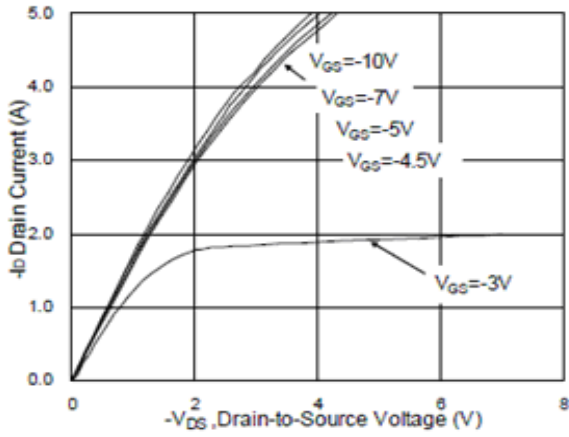


Fig 1 Output Characteristics

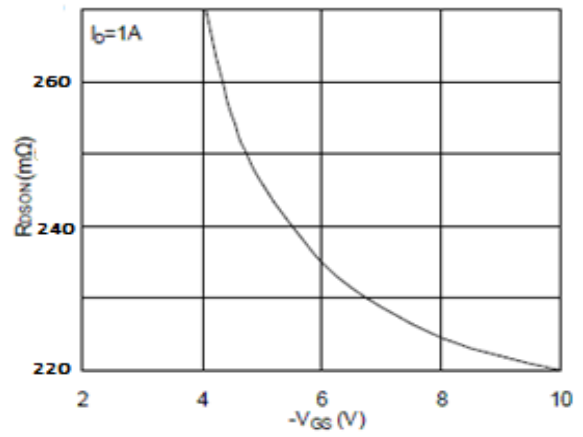


Fig. 2 On-Resistance vs Gate Source Voltage

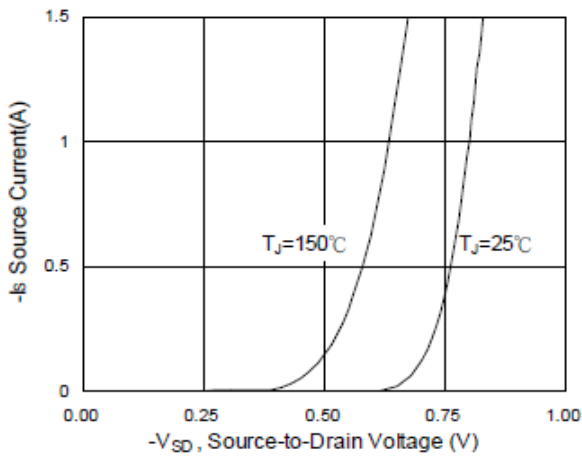


Fig 3 Source-Drain Forward Voltage

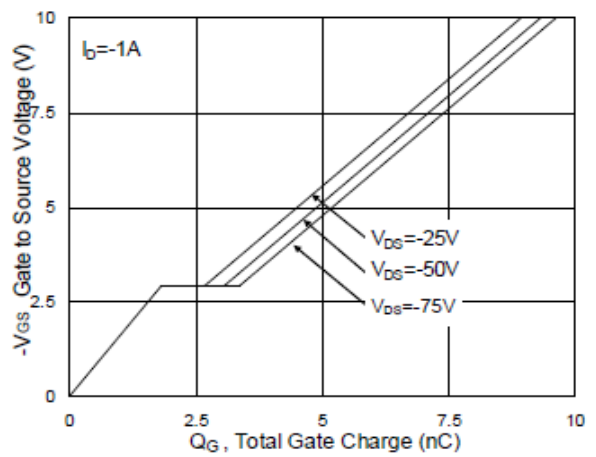


Fig. 4 Gate Charge

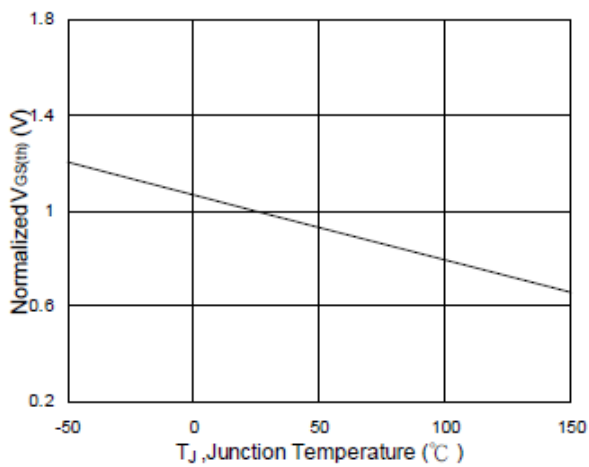


Fig. 5 Gate Voltage vs Junction temperature

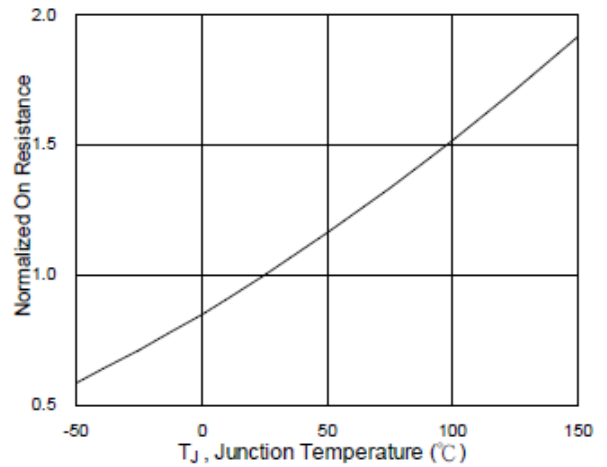


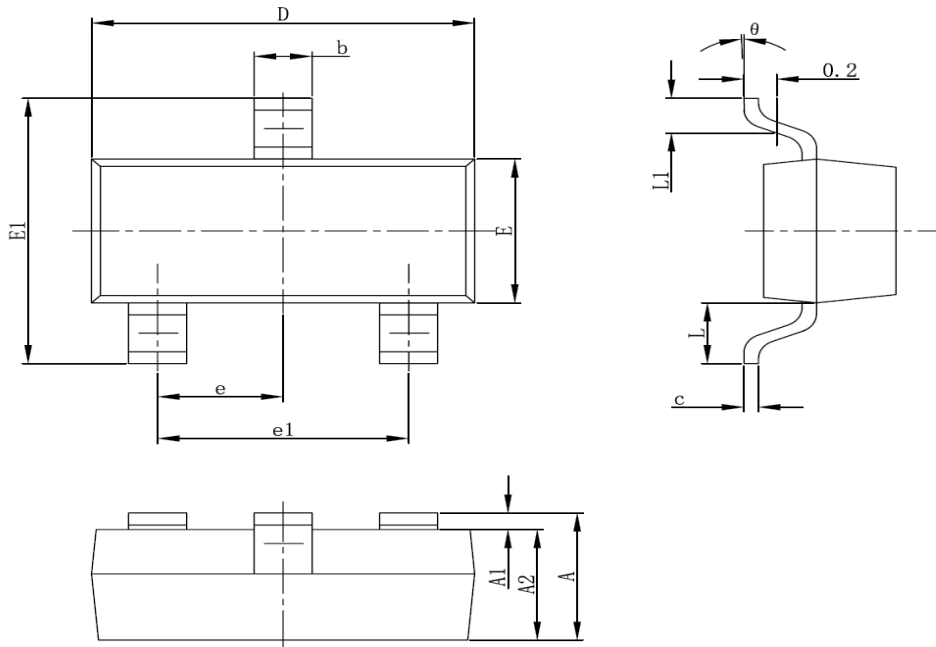
Fig. 6 On-Resistance vs Junction Temperature



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### SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°



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