SPP4437
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP4437 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP4437 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

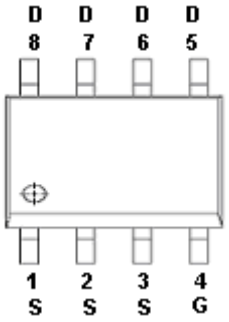
- MB/VGA/Vcore/PD Application
- DC/DC Power System
- Load Switch

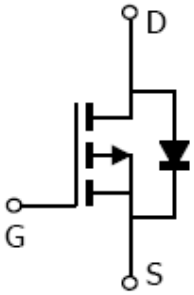
FEATURES

- -30V/-10A, $R_{DS(ON)}$=8.5mΩ@V_{GS}=-10V
- -30V/-8A, $R_{DS(ON)}$=14.5mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

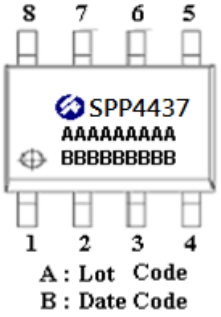
PIN CONFIGURATION

SOP-8





PART MARKING



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP4437S8RGB	SOP-8	SPP4437

※ SPP4437S8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	-13.5	A
	T_A=70℃		-10.8	
Pulsed Drain Current		I_{DM}	-50	A
Power Dissipation	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient (t≦10s)		$R_{\theta JA}$	70	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0		-2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V, T_J=100℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥-5V,V_{GS} =-10V			-100	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= -10V,I_D=-10A		7	8.5	mΩ
		V_{GS}=-4.5V,I_D=-8A		11.4	14.5	
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-3A		14		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS} =0V			-1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V, V_{GS}=-4.5V I_D= -10A		35		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			10.5		
Input Capacitance	C_{iss}	V_{DS}=-15VV_{GS}=0V f=1MHz		3300		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			280		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V, I_D=-1A,V_{GS}=-10V, R_G=6Ω		24.5		nS
	t_r			10.5		
Turn-Off Time	$t_{d(off)}$			156		
	t_f			50		

TYPICAL CHARACTERISTICS

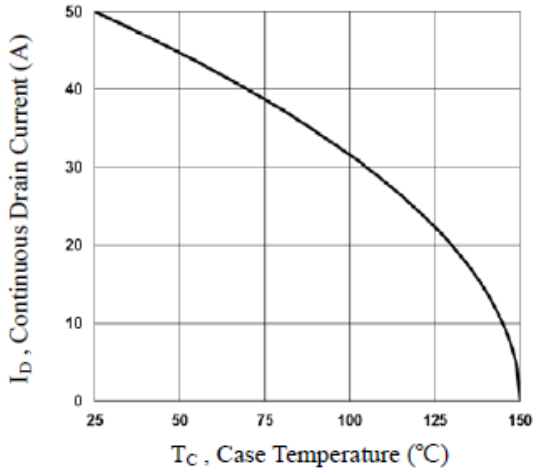


Fig.1 Continuous Drain Current vs. T_c

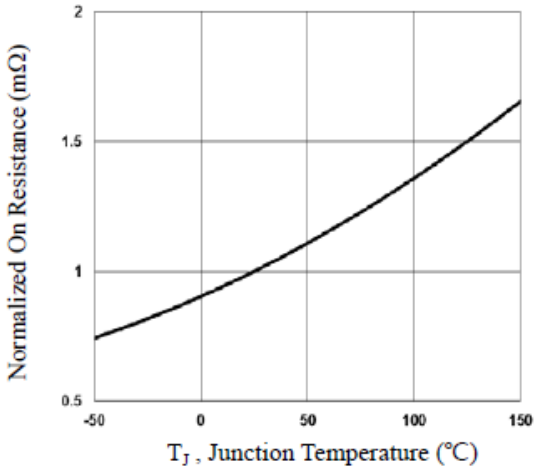


Fig.2 Normalized RDSON vs. T_J

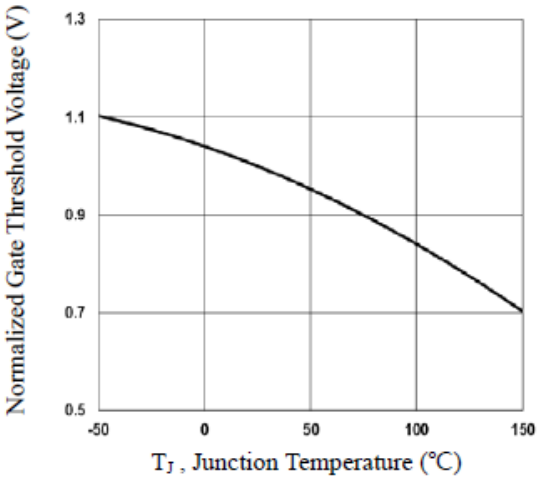


Fig.3 Normalized V_{th} vs. T_J

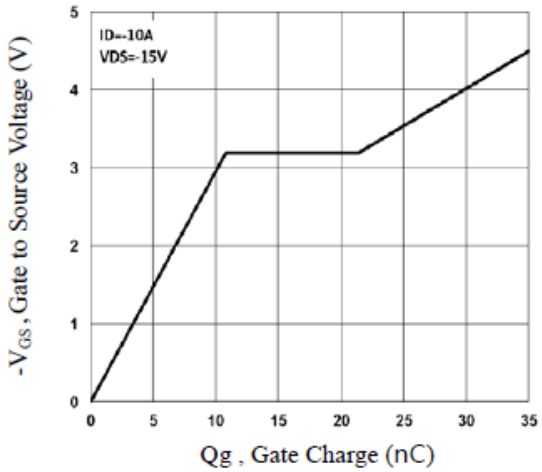


Fig.4 Gate Charge Waveform

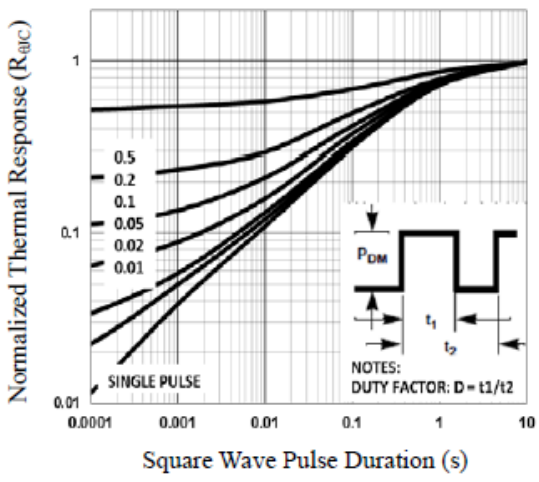


Fig.5 Normalized Transient Impedance

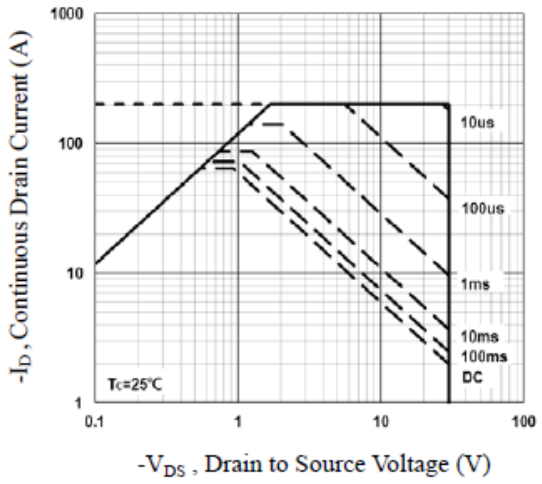
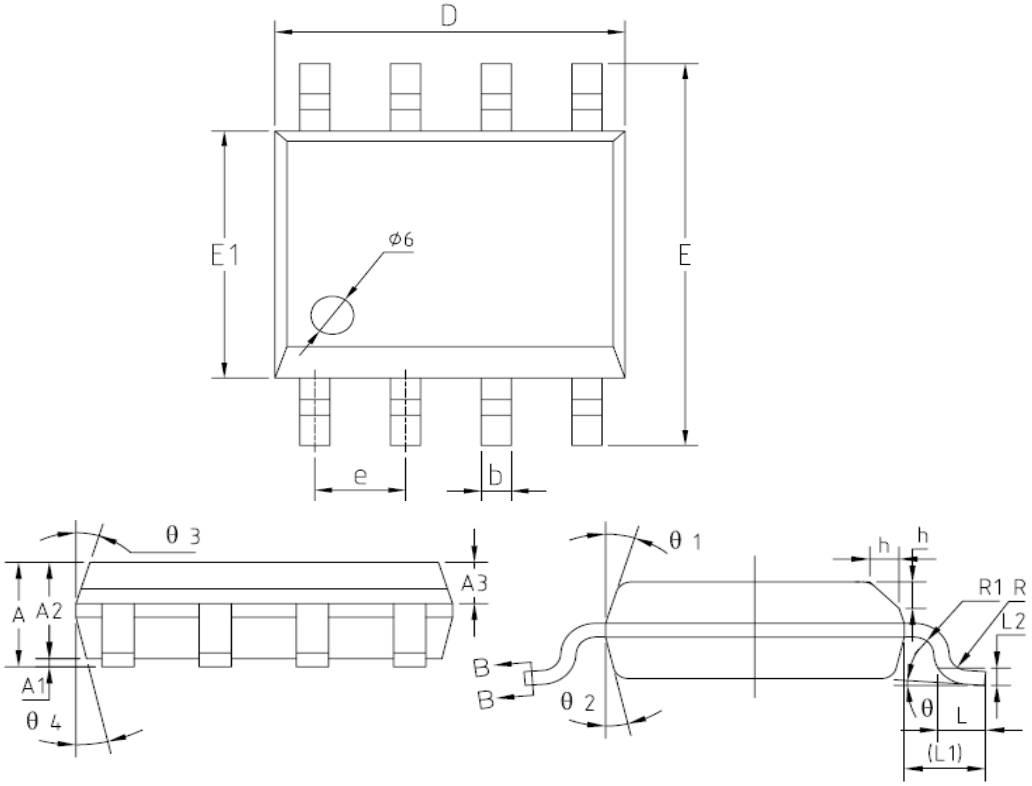


Fig.6 Maximum Safe Operation Area

SOP-8 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.35	--	1.75
A1	0.10	--	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.33	-	0.51
c	0.17	--	0.25
D	4.80	4.93	5.05
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	0.20
h	0.25	--	0.50
θ	0°	--	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°

SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan 115
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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