



SPP6241

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP6241 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

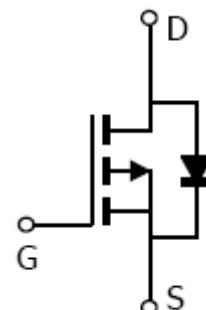
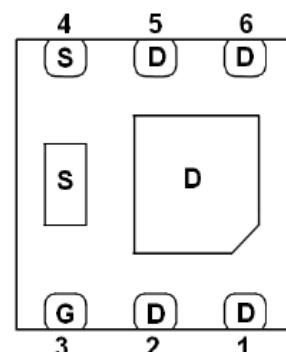
FEATURES

- ◆ -20V/-3.3 A,R_{DS(ON)}=45mΩ@V_{GS}=-4.5V
- ◆ -20V/-2.8 A,R_{DS(ON)}=55mΩ@V_{GS}=-2.5V
- ◆ -20V/-2.3 A,R_{DS(ON)}=65mΩ@V_{GS}=-1.8V
- ◆ Super high density cell design for extremely low R_{DS} (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ UDFN2X2-6L package design

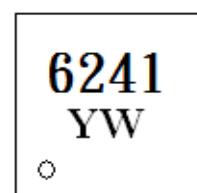
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(UDFN2X2-6L)



PART MARKING



Y : Year Code
W: Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP6241UDN6RGB	UDFN2X2-6L	6241YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP6241UDN6RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUT MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-20	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	ID	A
	T _A =70°C		
Pulsed Drain Current*	I _{DM}	-30	A
Continuous Source Current(Diode Conduction)	I _S	-1.6	A
Power Dissipation	T _A =25°C	P _D	W
	T _A =70°C		
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	65	°C/W

*Junction temperature limited.



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ELECTRICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)

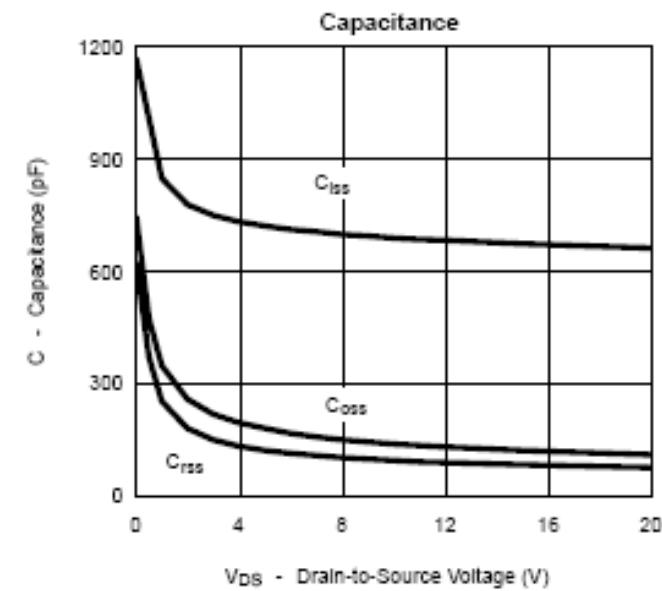
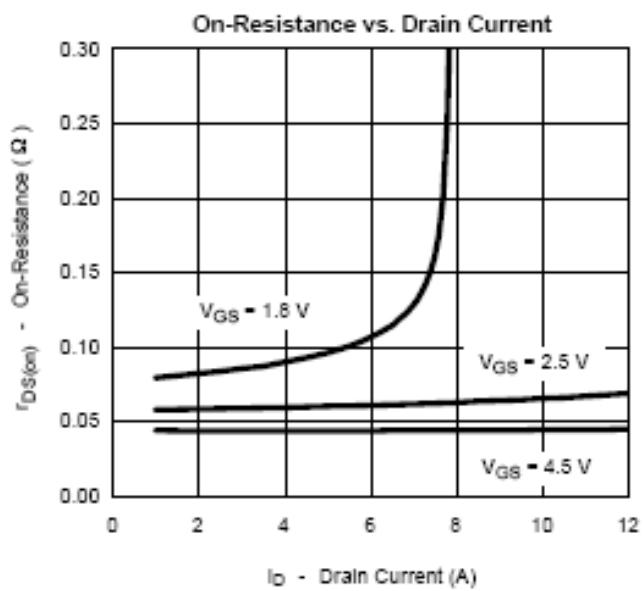
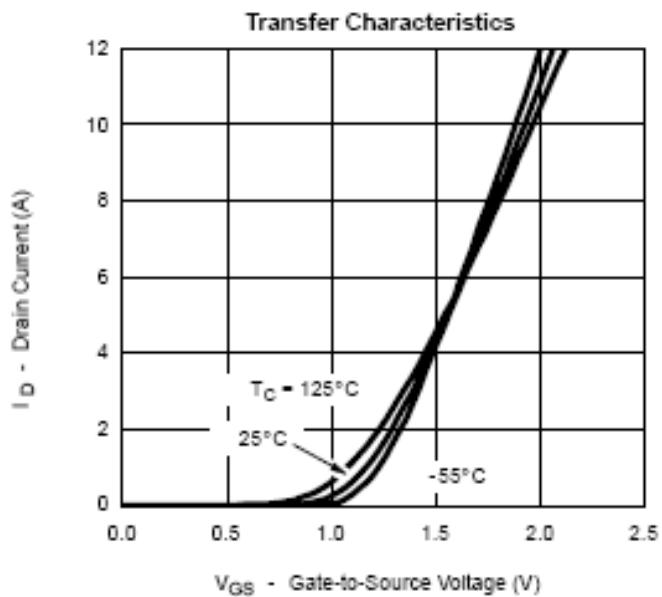
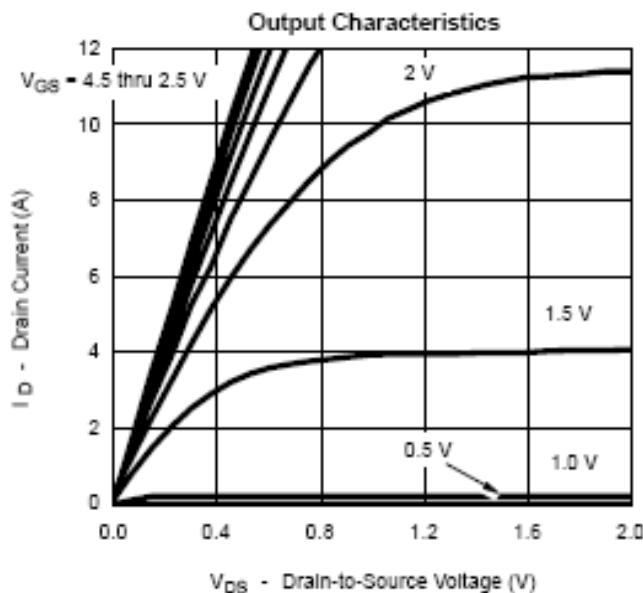
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=-250uA	-0.35		-0.9	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	
		V _{DS} =-20V, V _{GS} =0V T _J =55°C			-10	uA
On-State Drain Current	I _{D(on)}	V _{DS} ≤-5V, V _{GS} =-4.5V	-6			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =-4.5V, ID=-3.3A		0.036	0.045	
		V _{GS} =-2.5V, ID=-2.8A		0.045	0.055	Ω
		V _{GS} =-1.8V, ID=-2.3A		0.055	0.065	
Forward Transconductance	g _{fs}	V _{DS} =-5.0V, ID=-3.3A		3		S
Diode Forward Voltage	V _{SD}	I _S =-1.6A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-6V, V _{GS} =-4.5V ID=-3.3A		8	13	
Gate-Source Charge	Q _{gs}			1.2		nC
Gate-Drain Charge	Q _{gd}			2.2		
Input Capacitance	C _{iss}	V _{DS} =-6V, V _{GS} =0V f=1MHz		700		
Output Capacitance	C _{oss}			160		pF
Reverse Transfer Capacitance	C _{rss}			120		
Turn-On Time	t _{d(on)}	V _{DD} =-6V, R _L =6Ω ID=-1.0A, V _{GEN} =-4.5V R _G =6Ω		15	25	
	t _r			35	55	nS
Turn-Off Time	t _{d(off)}			60	90	
	t _f			40	60	



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TYPICAL CHARACTERISTICS

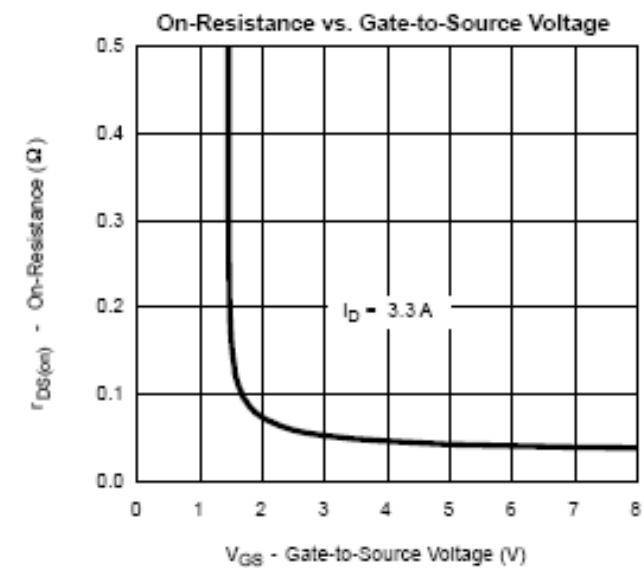
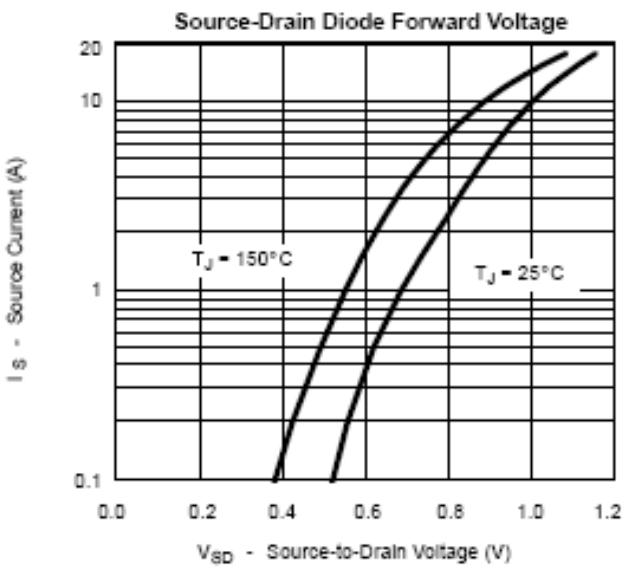
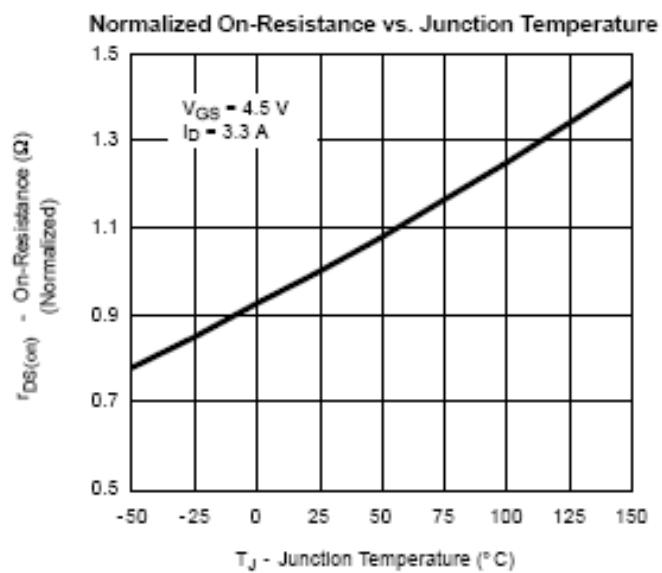
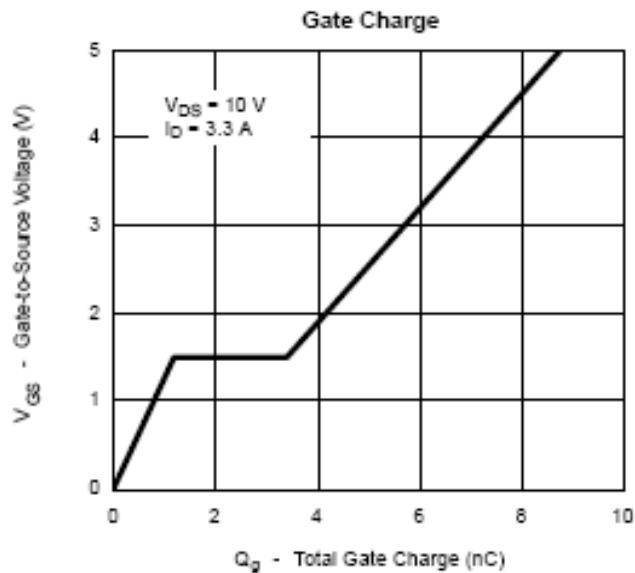




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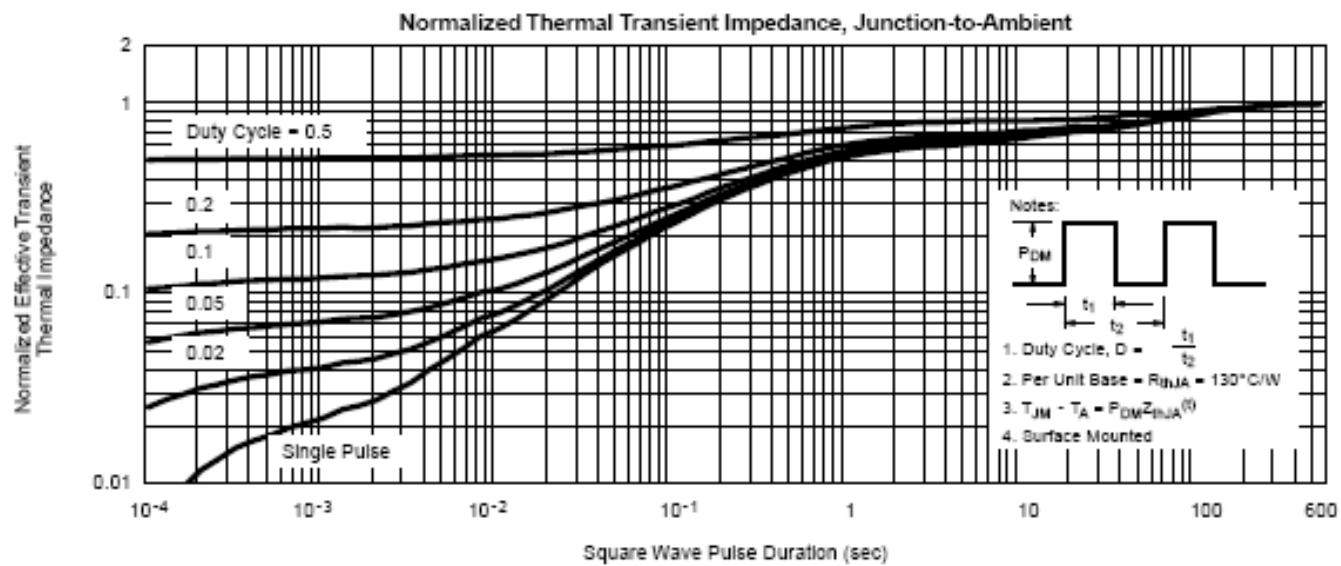
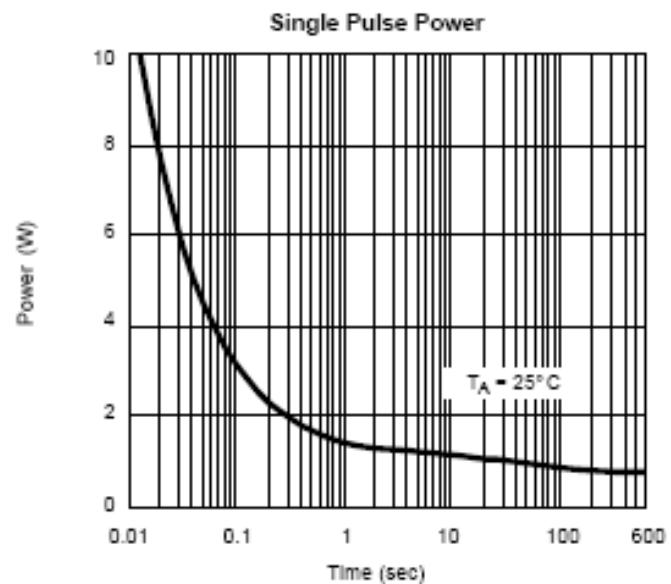
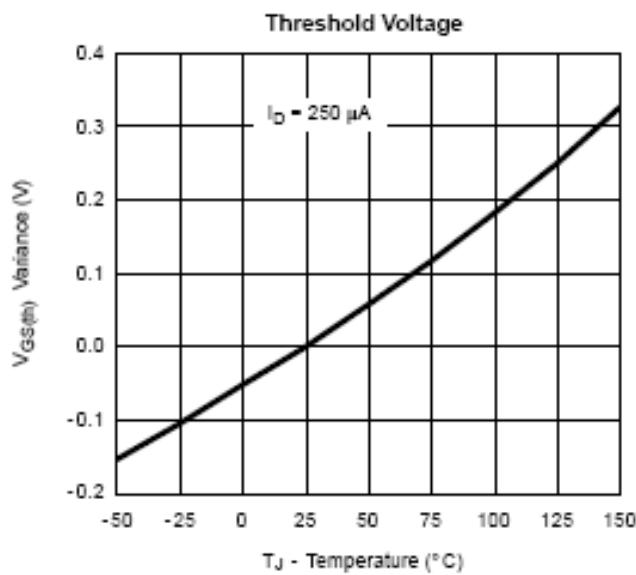




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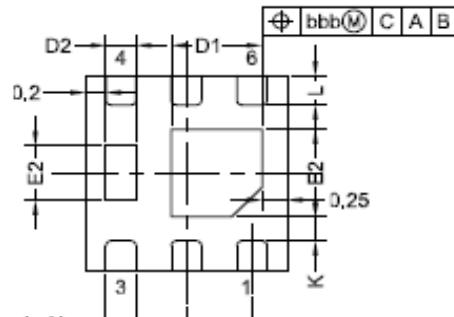




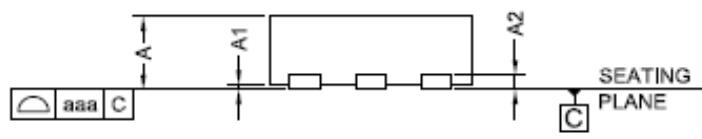
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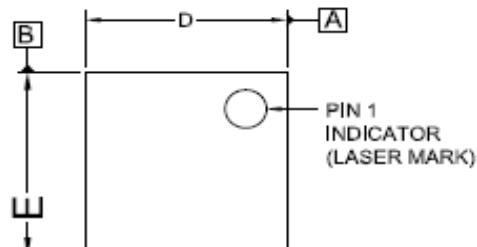
UDFN2X2-6L PACKAGE OUTLINE



BOTTOM VIEW



SIDE VIEW



TOP VIEW

SYMBOL	MIN	TYP	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.152REF,		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D1	0.80	0.90	1.00
D2	0.25	0.30	0.35
E	1.95	2.00	2.05
E1	0.80	0.90	1.00
E2	0.46	0.56	0.66
g	0.65BSC		
L	0.25	0.30	0.35
J	0.40BSC		
K	0.20MIN		
N	6		
aaa	0.08		
bbb	0.10		



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