



SPP8525

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8525 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

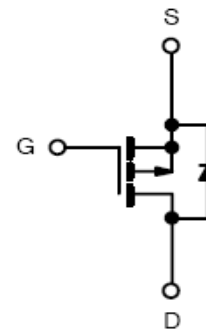
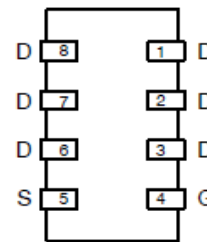
FEATURES

- ◆ -20V/-7.2 A, $R_{DS(ON)}=40m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-5.2 A, $R_{DS(ON)}=52m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-3.6 A, $R_{DS(ON)}=70m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x2-8L package design

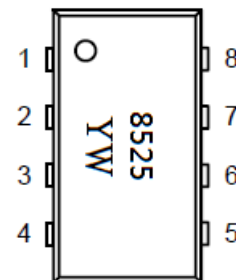
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(PPAK3x2-8L)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	D	Drain
4	G	Gate
5	S	Source
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8525DN8RGB	PPAK3x2-8L	8525YW

※ SPP8525DN8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-7.6	A
		TA=70°C	-5.4	
Pulsed Drain Current	I _{DM}	-30	A	
Continuous Source Current(Diode Conduction)	I _S	-2.3	A	
Power Dissipation	P _D	TA=25°C	2.8	W
		TA=70°C	1.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	70	°C/W	



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ELECTRICAL CHARACTERISTICS

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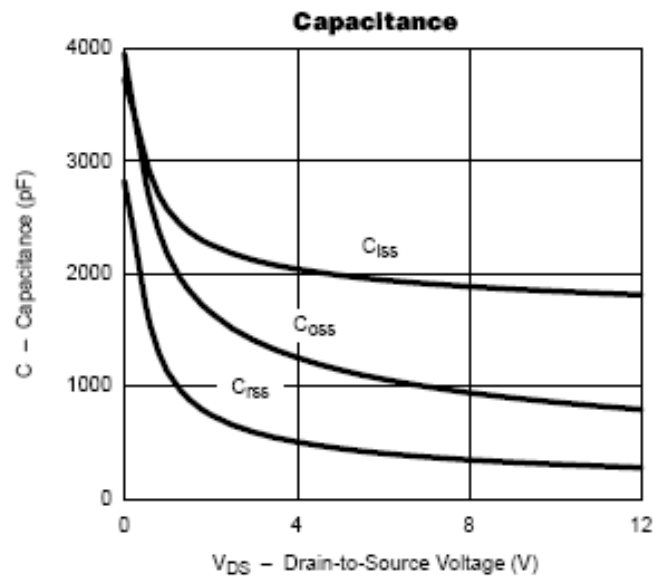
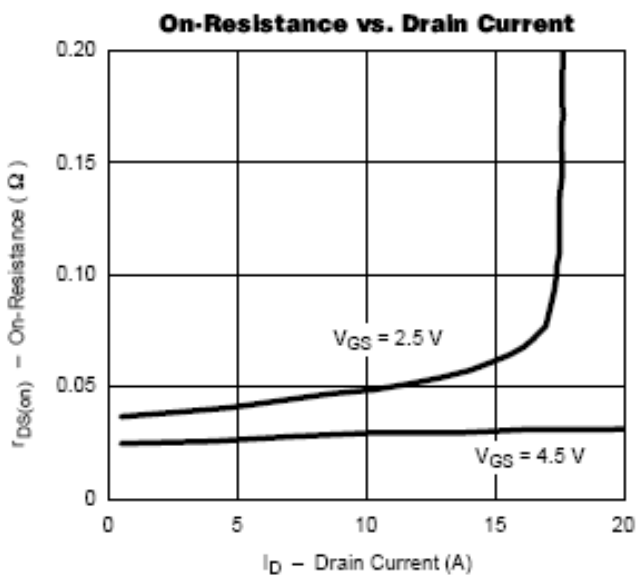
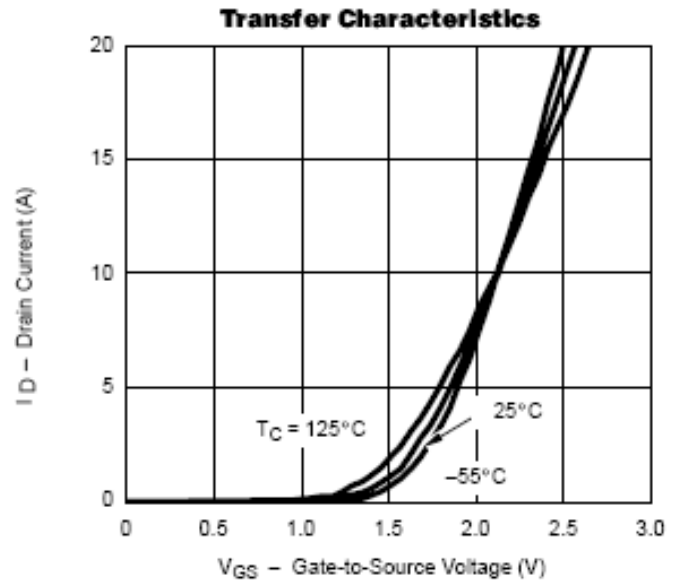
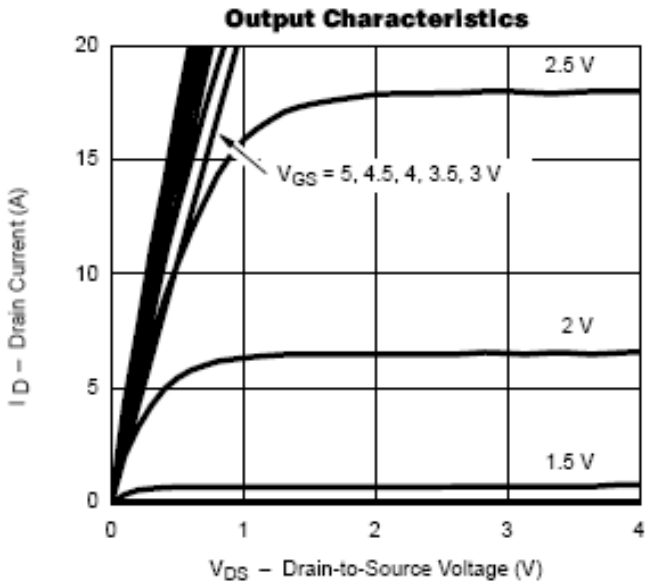
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.35		-0.9	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V			-1	uA
		V _{DS} =-16V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =- 4.5V, I _D =-7.2A		30	40	mΩ
		V _{GS} =- 2.5V, I _D =-5.2A		40	52	
		V _{GS} =- 1.8V, I _D =-3.6A		55	70	
Forward Transconductance	g _{fs}	V _{DS} =-5.0V, I _D =-6.2A		14		S
Diode Forward Voltage	V _{SD}	I _S =-2.5A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-10V, V _{GS} =-4.5V I _D =-6.4A		20	25	nC
Gate-Source Charge	Q _{gs}			4.5		
Gate-Drain Charge	Q _{gd}			8.0		
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V f=1MHz		700		pF
Output Capacitance	C _{oss}			160		
Reverse Transfer Capacitance	C _{rss}			120		
Turn-On Time	t _{d(on)}	V _{DD} =-10V, R _L =6Ω I _D =-1.0A, V _{GEN} =-4.5V R _G =6Ω		20	30	ns
	t _r			40	65	
Turn-Off Time	t _{d(off)}			90	120	
	t _f			70	90	



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TYPICAL CHARACTERISTICS

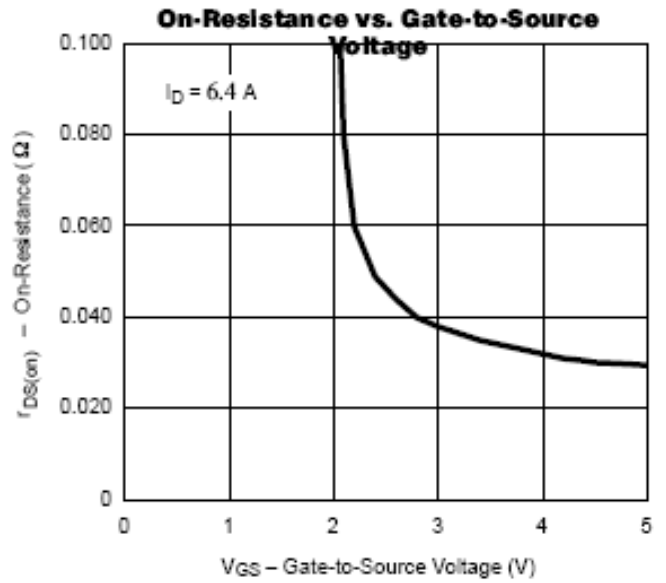
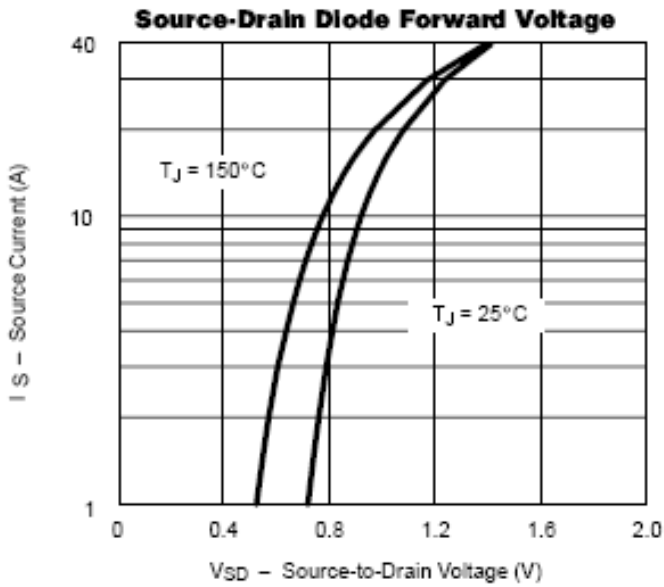
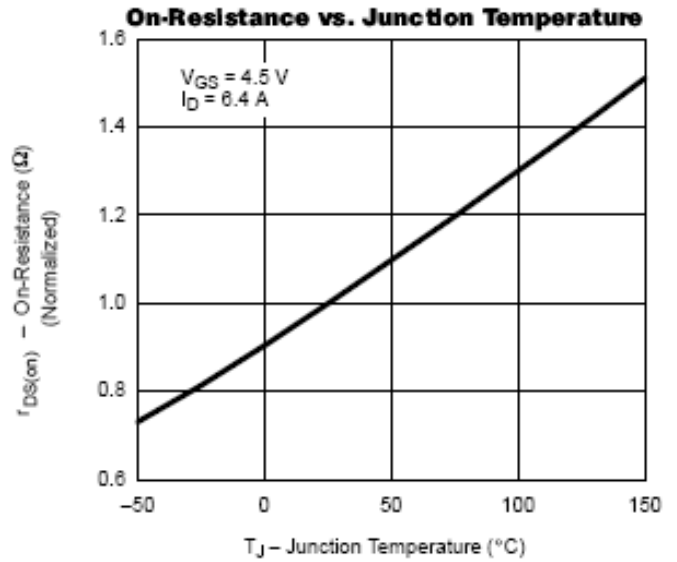
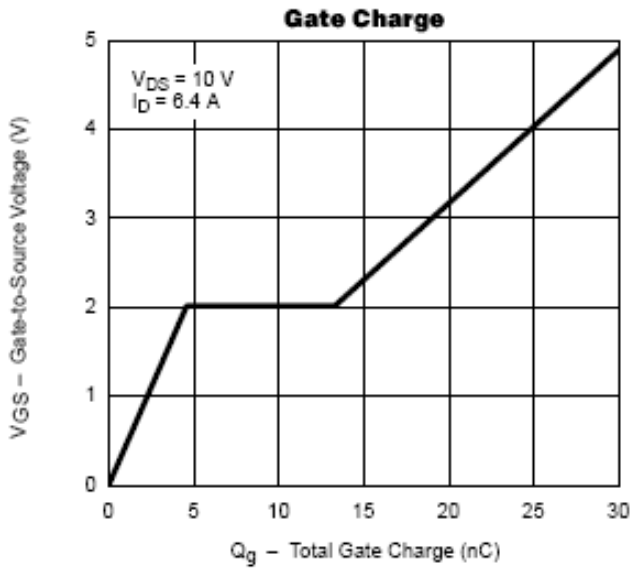




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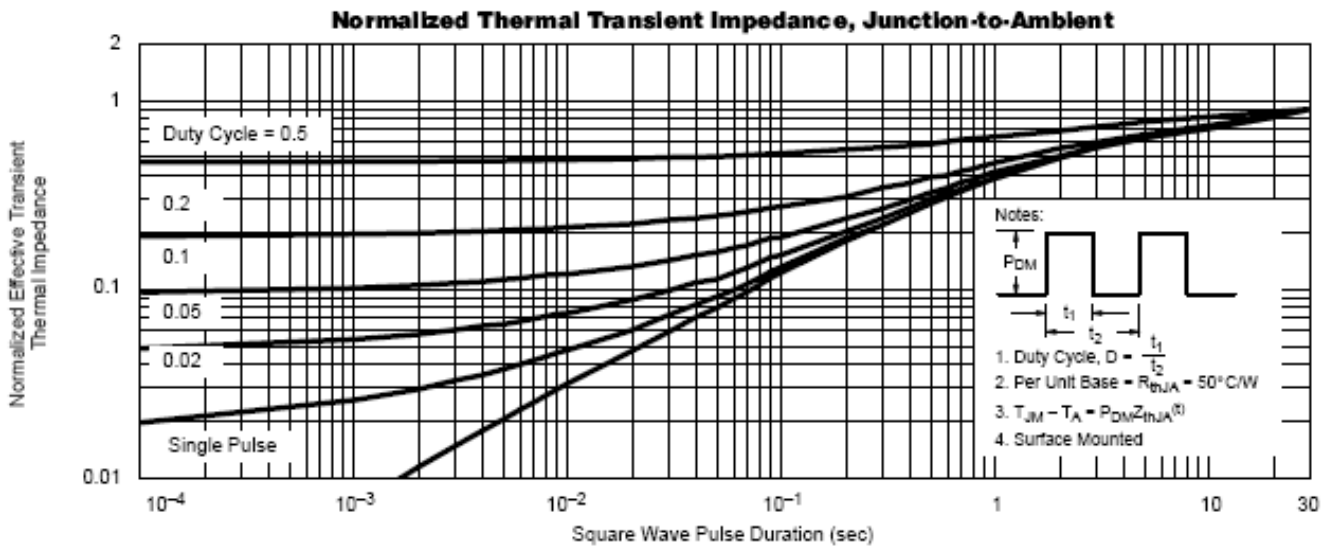
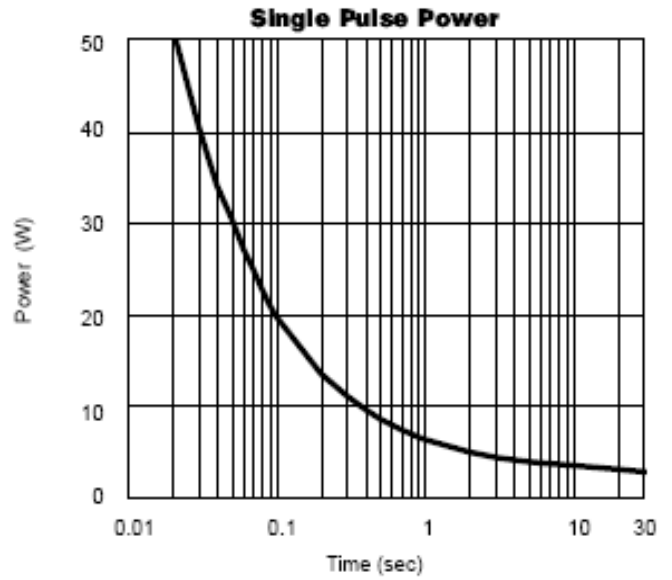
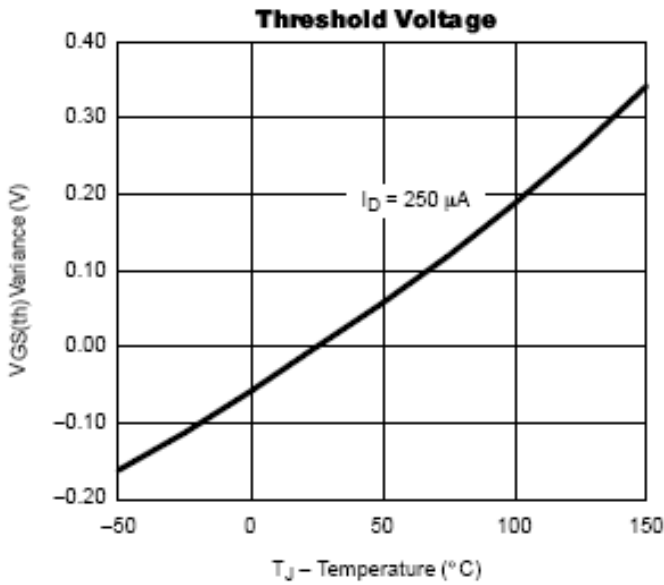
TYPICAL CHARACTERISTICS





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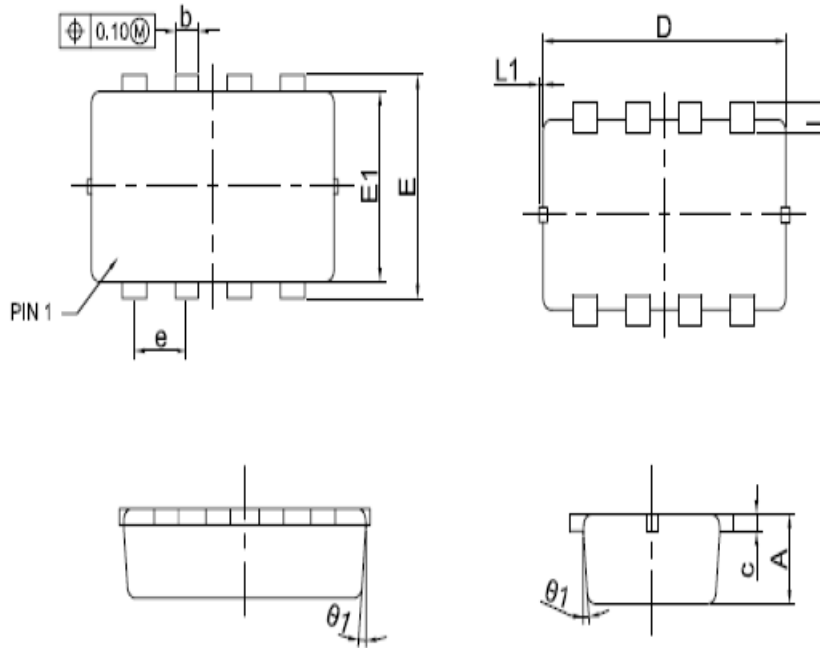




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PPAK3X2-8L PACKAGE OUTLINE



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0,70	0,80	0,90
b	0,24	0,30	0,35
c	0,08	0,15	0,20
D	2,90	3,00	3,05
E	1,90	2,00	2,10
E1	1,60	1,70	1,75
e	0,65 BCS		
L	0,20	0,275	0,400
L1	0	—	0,100
θ_1	0°	5°	8°



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