



SPP8637

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8637 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP8637 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

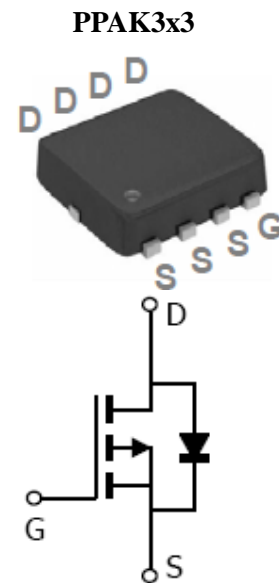
FEATURES

- ◆ -30V/-30A, $R_{DS(ON)}=8.5m\Omega@V_{GS}=-10V$
- ◆ -30V/-20A, $R_{DS(ON)}=14.5m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK3x3 package design

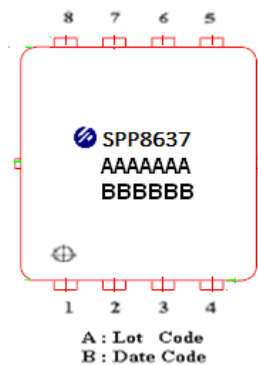
APPLICATIONS

- MB/VGA/Vcore/PD Application
- DC/DC Power System
- Load Switch

PIN CONFIGURATION



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PPAK3x3 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8637DN8RGB	PPAK3x3	SPP8637

※ SPP8637DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	-30	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^{\circ}\text{C}$	-50
		$T_A=100^{\circ}\text{C}$	-32
Pulsed Drain Current	I_{DM}	-200	A
Power Dissipation	P_D	59	W
Operating Junction Temperature	T_J	150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient ($t \leq 10\text{s}$)	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V, T_J=100^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq -5V, V_{GS}=-10V$			-100	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-30A$		7	8.5	mΩ
		$V_{GS}=-4.5V, I_D=-20A$		11.4	14.5	
Gate Resistance	R_g	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		8.5	12	Ω
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-3A$		14		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-4.5V$ $I_D=-10A$		35		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			10.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		3300		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			280		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V,$ $I_D=-1A, V_{GS}=-10V, R_G=6\Omega$		24.5		nS
	t_r			10.5		
Turn-Off Time	$t_{d(off)}$			156		
	t_f			50		



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TYPICAL CHARACTERISTICS

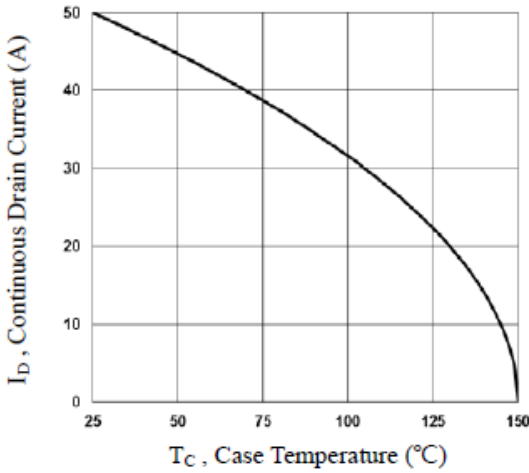


Fig.1 Continuous Drain Current vs. T_C

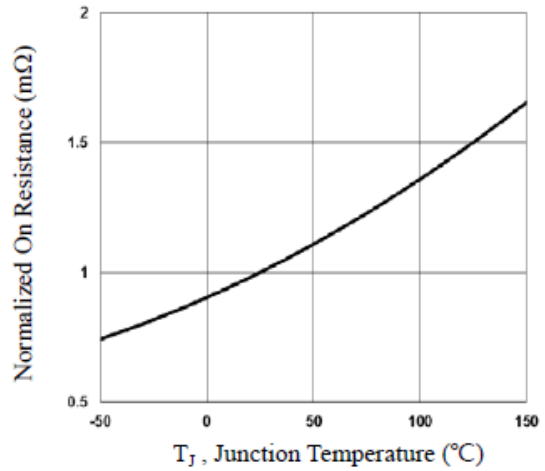


Fig.2 Normalized $R_{DS(on)}$ vs. T_J

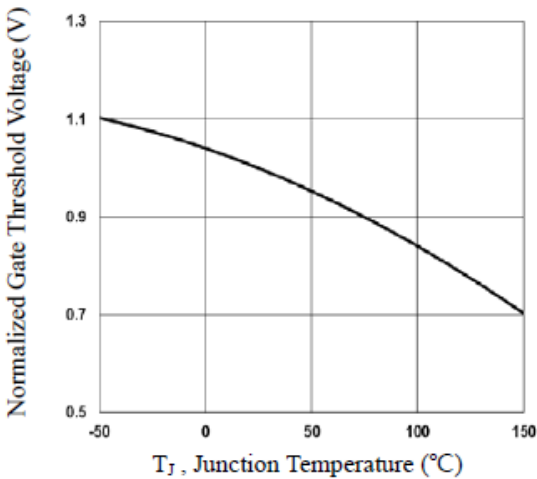


Fig.3 Normalized V_{th} vs. T_J

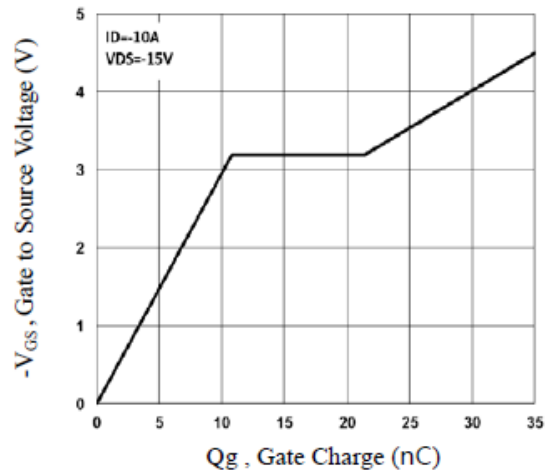


Fig.4 Gate Charge Waveform

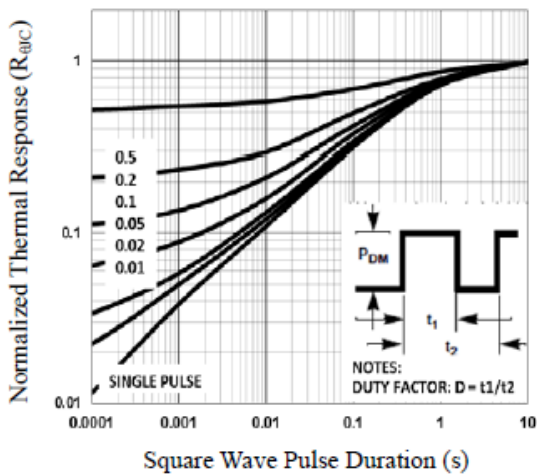


Fig.5 Normalized Transient Impedance

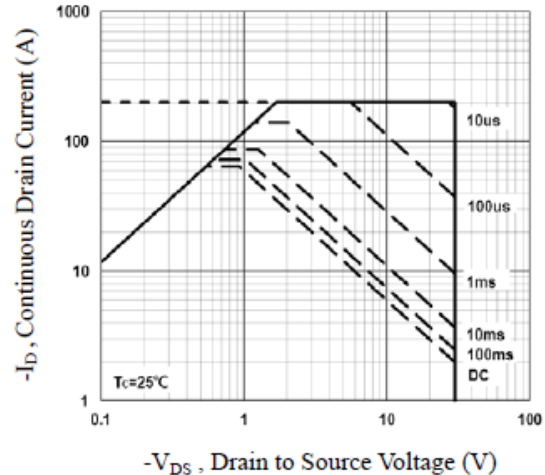


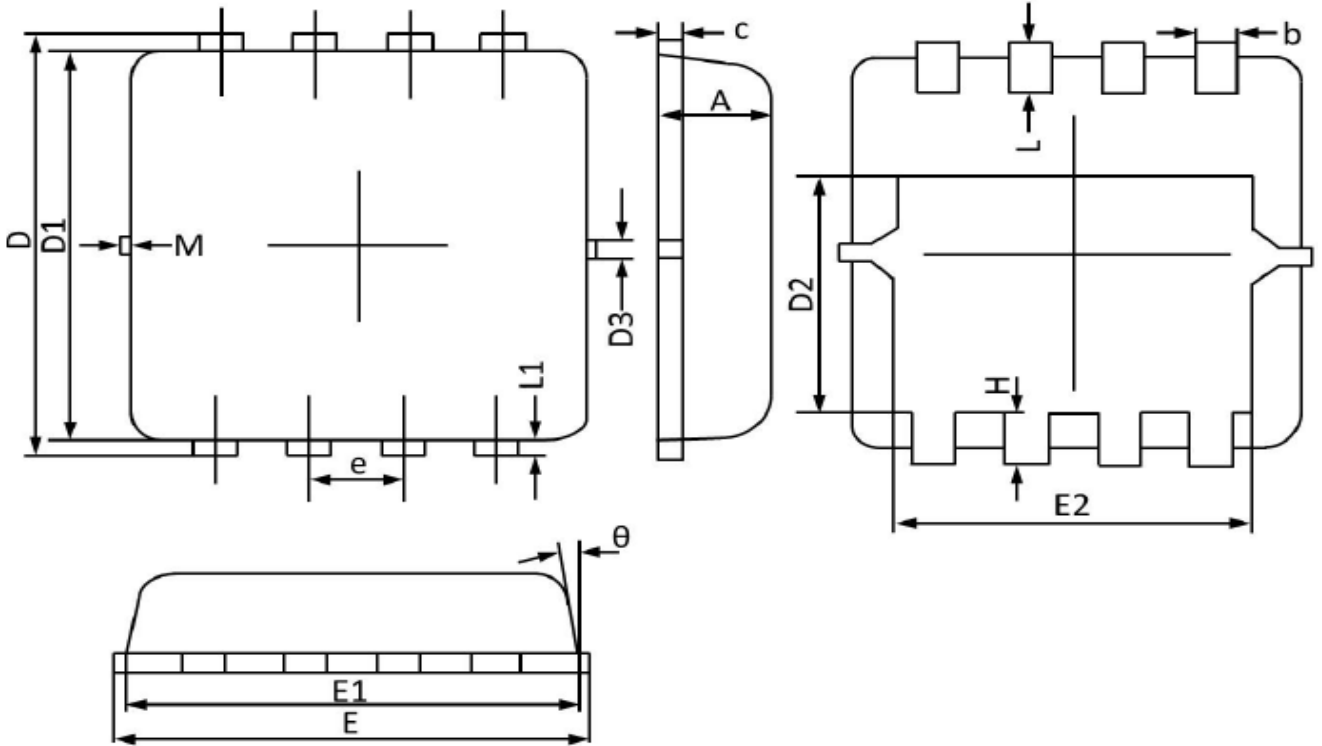
Fig.6 Maximum Safe Operation Area



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PPAK3x3 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 REF		0.005 REF	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 BSC		0.026 BSC	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 REF		0.005 REF	
theta	0°	12°	0°	12°
M	0.150 REF		0.006 REF	



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