



SPP8835

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8835 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP8835 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low RDS(ON) and fast switching speed.

FEATURES

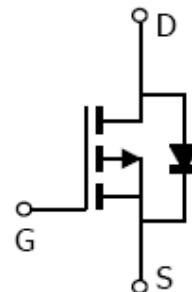
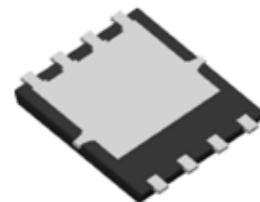
- ◆ -30V/-30A, $R_{DS(ON)}=3.3m\Omega$ @ $V_{GS}=-10V$
- ◆ -30V/-20A, $R_{DS(ON)}=5m\Omega$ @ $V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5X6 package design

APPLICATIONS

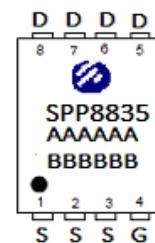
- High Frequency Synchronous Buck Converter
- DC/DC Power System
- Load Switch

PIN CONFIGURATION

PPAK5X6



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PPAK5X6 PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8835DN8RGB	PPAK5X6	SPP8835

※ SPP8835DN8RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current TA=25°C	I _D	-100	A
TA=100°C		-82	
Pulsed Drain Current	I _{DM}	-400	A
Avalanche Current	I _{AS}	-80	A
Single Pulse Avalanche Energy	E _{AS}	320	mJ
Power Dissipation	P _D	83	W
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient (t≤10s)	R _{θJA}	55	°C/W



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=-250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _D =V _{GS} , ID=-250uA	-1.2		-2.5	
Gate Leakage Current	I _{GSS}	V _D =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _D =-30V, V _{GS} =0V			-1	
		V _D =-24V, V _{GS} =0V, T _J =100°C			-10	uA
On-State Drain Current	I _{D(on)}	V _D ≥-5V, V _{GS} =-10V			-100	A
Drain-Source On-Resistance	R _{D(on)}	V _{GS} = -10V, ID=-30A		2.6	3.3	
		V _{GS} =-4.5V, ID=-20A		3.8	5	mΩ
Forward Transconductance	g _f s	V _D =-10V, ID=-3A		20		S
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1	V
Dynamic						
Total Gate Charge	Q _g	V _D =-24V, V _{GS} =-10V ID= -10A		148	210	nC
Gate-Source Charge	Q _{gs}			22		
Gate-Drain Charge	Q _{gd}			32		
Input Capacitance	C _{iss}	V _D =-25V, V _{GS} =0V f=1MHz		7950		pF
Output Capacitance	C _{oss}			982		
Reverse Transfer Capacitance	C _{rss}			500		
Turn-On Time	t _{d(on)}	V _D =-15V, ID=-10A, V _{GS} =-10V, R _G =5Ω		17	34	nS
	t _r			61	120	
Turn-Off Time	t _{d(off)}			200	400	
	t _f			113	220	



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TYPICAL CHARACTERISTICS

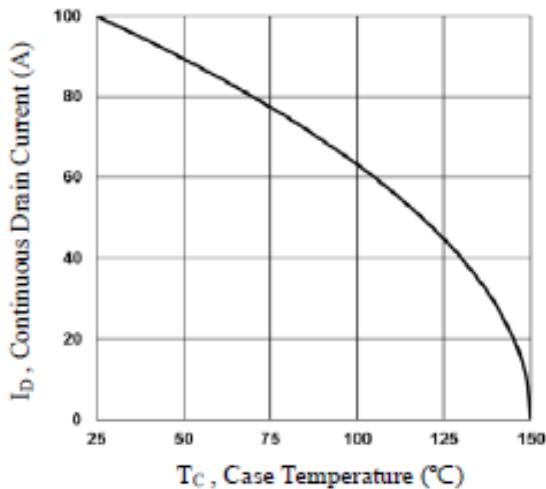


Fig.1 Continuous Drain Current vs. T_c

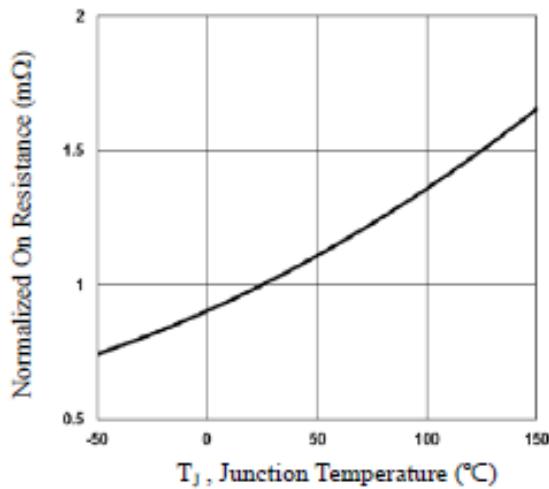


Fig.2 Normalized RD_{SON} vs. T_j

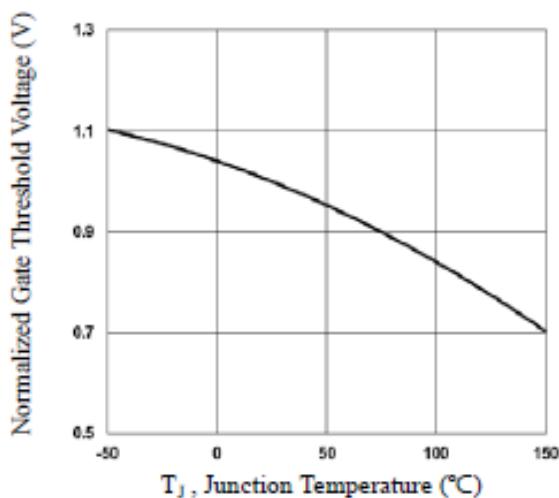


Fig.3 Normalized V_{th} vs. T_j

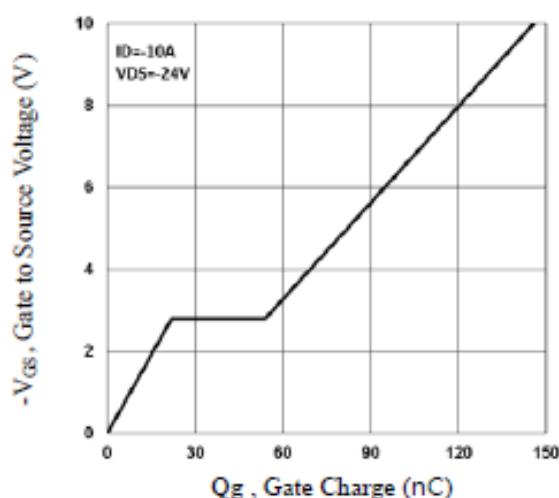
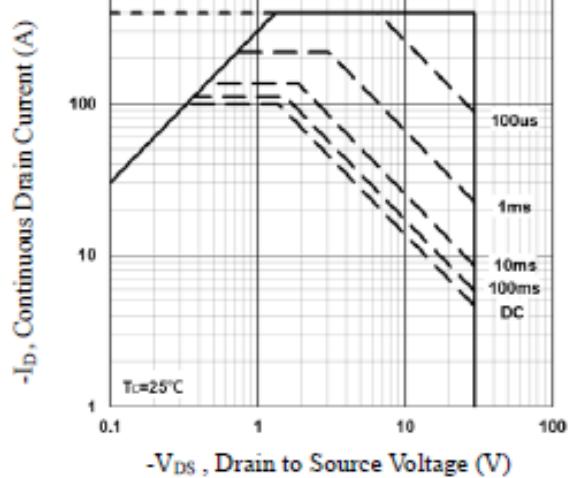
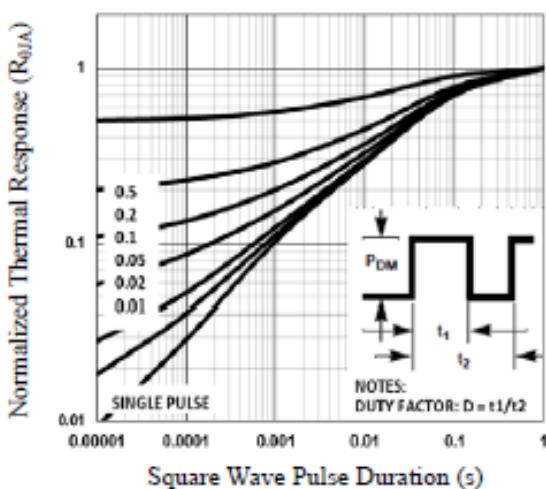


Fig.4 Gate Charge Waveform

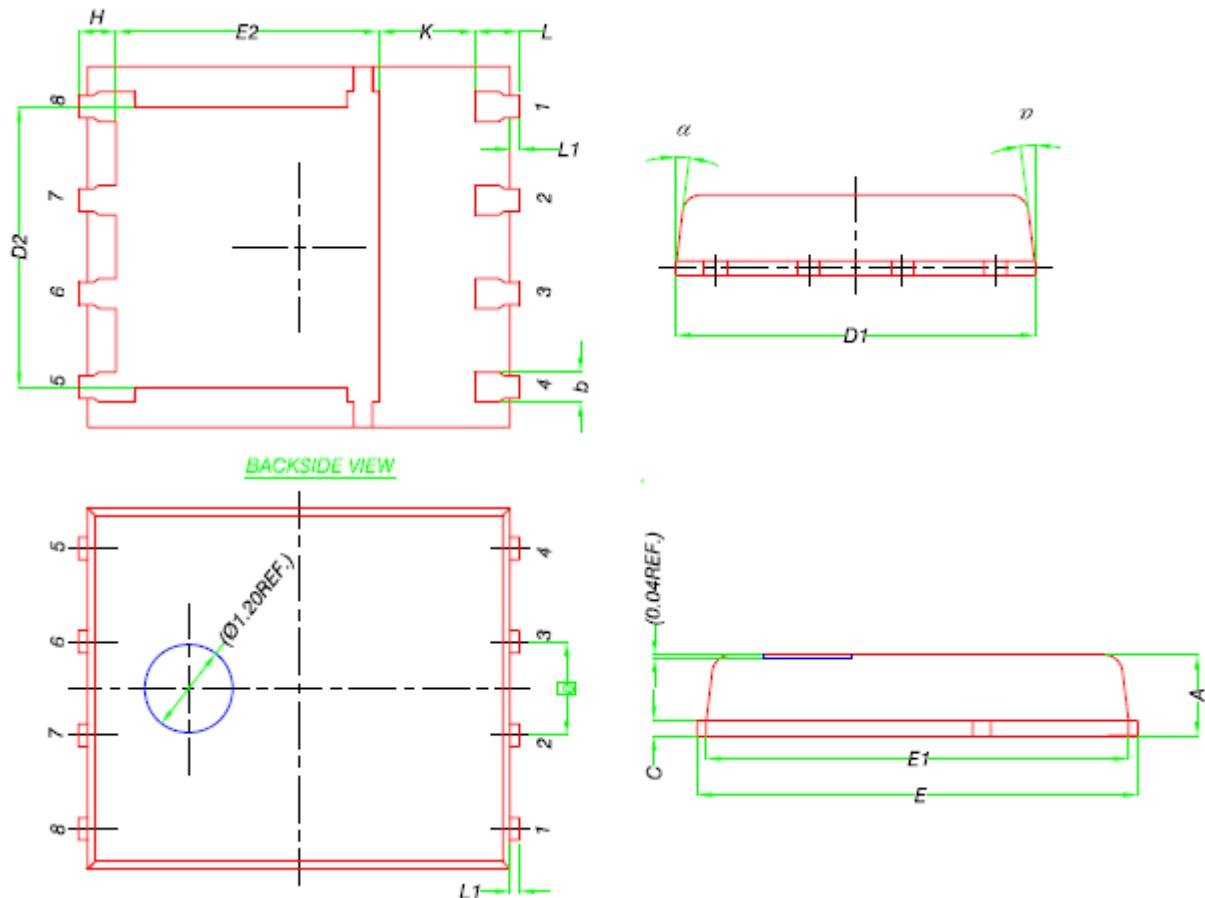




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PPAK5X6 PACKAGE OUTLINE



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.61	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
[e]	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
alpha	0°	-	12°



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