



SPN7400

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN7400 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

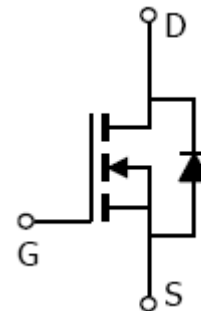
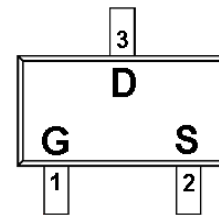
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

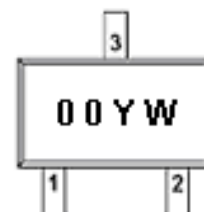
FEATURES

- ◆ 30V/2.8A, $R_{DS(ON)}=77m\Omega@V_{GS}=10V$
- ◆ 30V/2.3A, $R_{DS(ON)}=85m\Omega@V_{GS}=4.5V$
- ◆ 30V/1.5A, $R_{DS(ON)}=110m\Omega@V_{GS}=2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-323 (SC-70) package design

PIN CONFIGURATION (SOT-323 ; SC-70)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN7400S32RG	SOT-323	00YW
SPN7400S32RGB	SOT-323	00YW

- ※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)
- ※ SPN7400S32RG : Tape Reel ; Pb – Free
- ※ SPN7400S32RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	30	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	2.8	A
		TA=70°C	2.3	
Pulsed Drain Current	I _{DM}	10	A	
Continuous Source Current(Diode Conduction)	I _S	1.25	A	
Power Dissipation	P _D	TA=25°C	0.33	W
		TA=70°C	0.21	
Operating Junction Temperature	T _J	150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W	



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ELECTRICAL CHARACTERISTICS

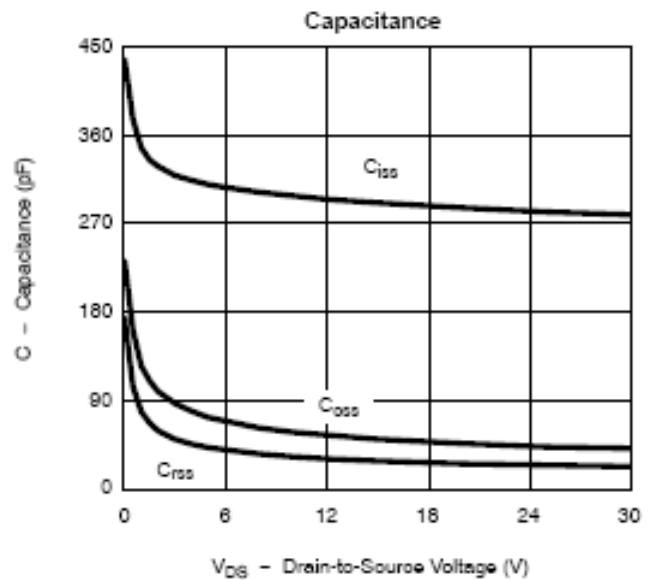
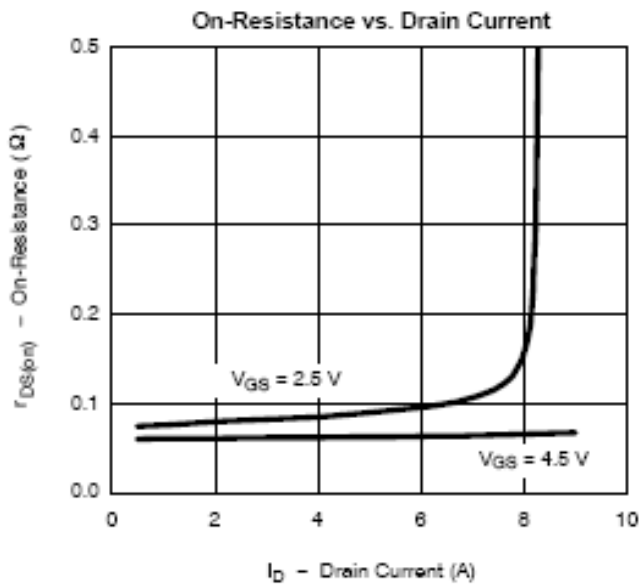
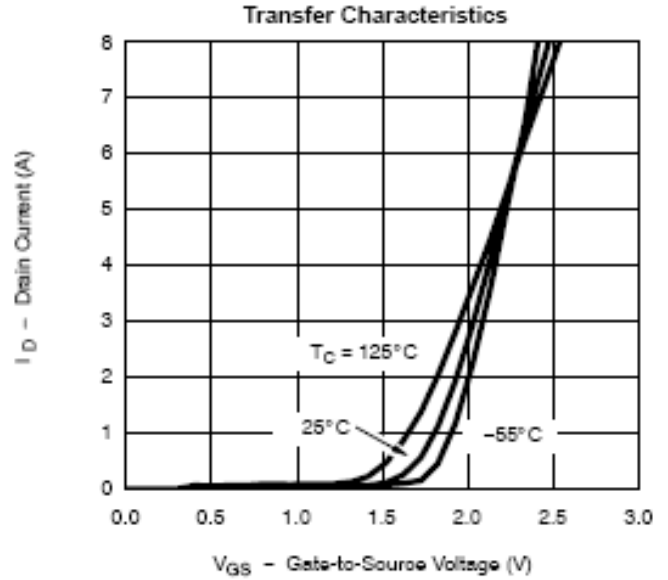
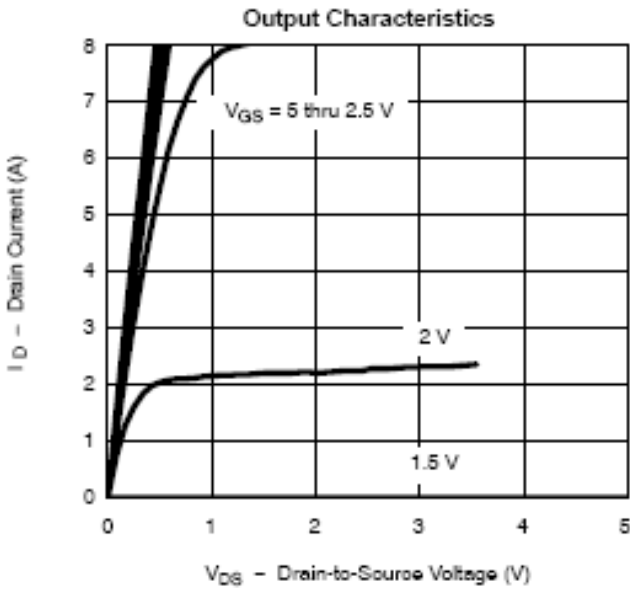
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.6		
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=1.0V$			1	uA	
		$V_{DS}=24V, V_{GS}=0.0V$ $T_J=55^\circ C$			10		
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 4.5V, V_{GS}=10V$	6			A	
		$V_{DS} \geq 4.5V, V_{GS}=4.5V$	4				
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D=2.8A$		0.062	0.077	Ω	
		$V_{GS} = 4.5V, I_D=2.3A$		0.070	0.085		
		$V_{GS} = 2.5V, I_D=1.5A$		0.095	0.110		
Forward Transconductance	g_{fs}	$V_{DS}=4.5V, I_D=2.8A$		4.6		S	
Diode Forward Voltage	V_{SD}	$I_S=1.25A, V_{GS}=0V$		0.82	1.2	V	
Dynamic							
Total Gate Charge	Q_g	$V_{DS}=15, V_{GS}=4.5V$ $I_D=2.0A$		4.2	6	nC	
Gate-Source Charge	Q_{gs}			0.6			
Gate-Drain Charge	Q_{gd}			1.5			
Input Capacitance	C_{iss}	$V_{DS}=15, V_{GS}=0V$ $f = 1MHz$		350		pF	
Output Capacitance	C_{oss}			55			
Reverse Transfer Capacitance	C_{rss}			41			
Turn-On Time	$t_{d(on)}$	$V_{DD}=15, R_L=10\Omega$ $V_{GEN}=10V, R_G=3\Omega$		2.5		ns	
	t_r			2.5			
Turn-Off Time	$t_{d(off)}$				20		
	t_f				4		



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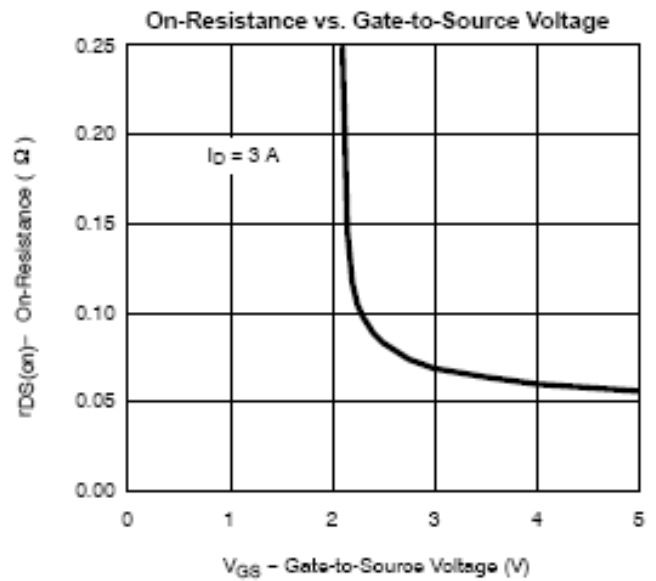
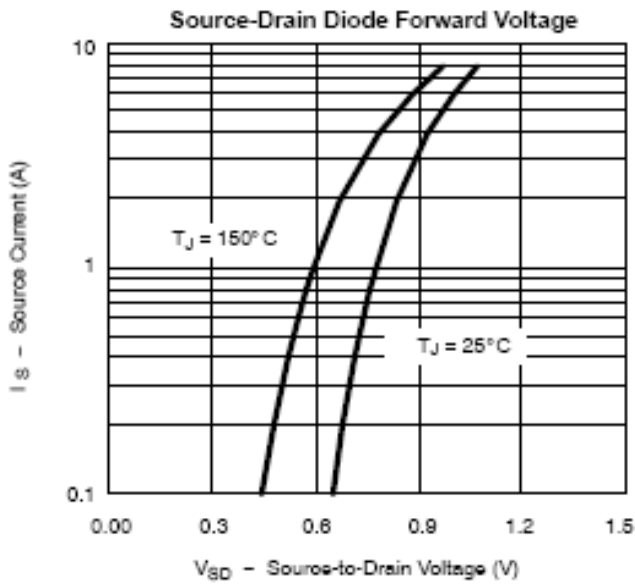
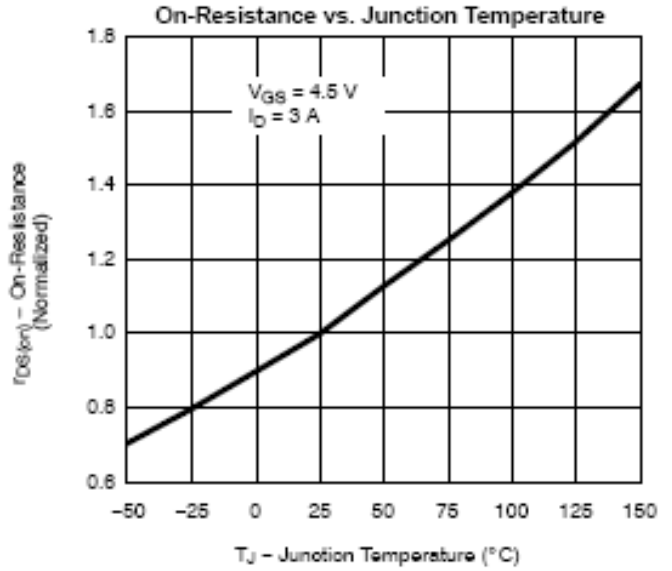
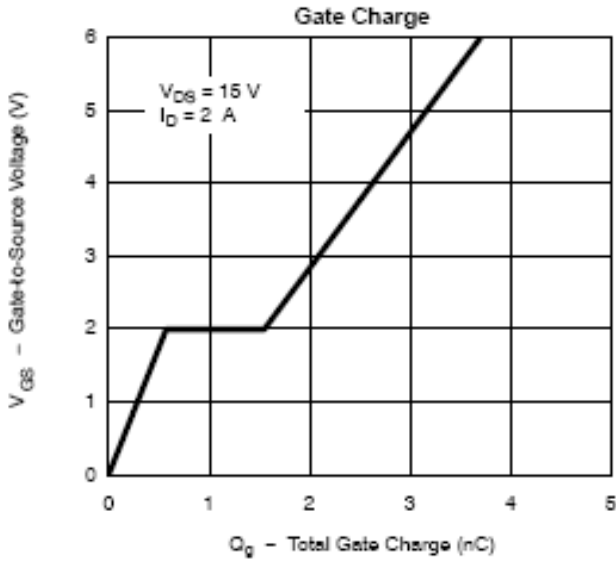
TYPICAL CHARACTERISTICS





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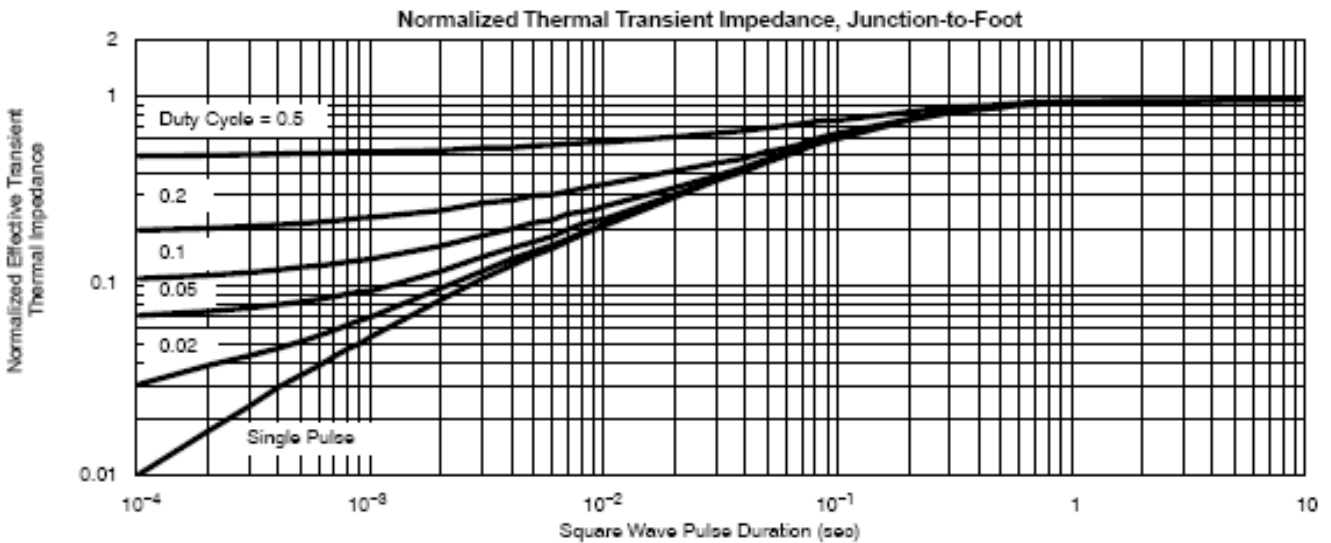
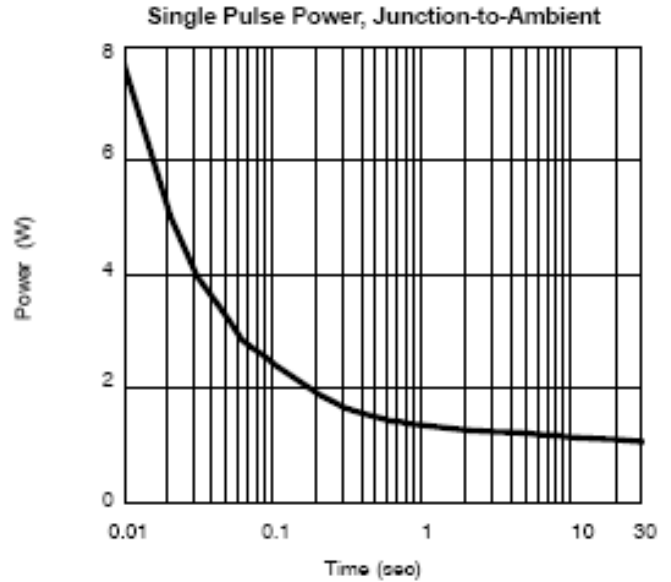
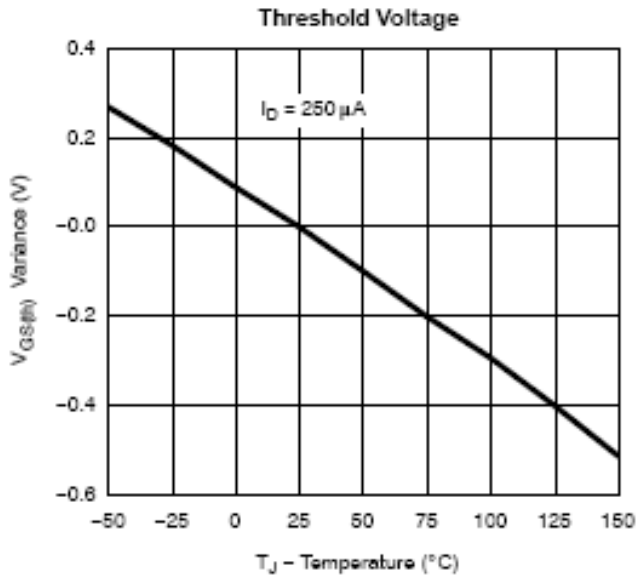
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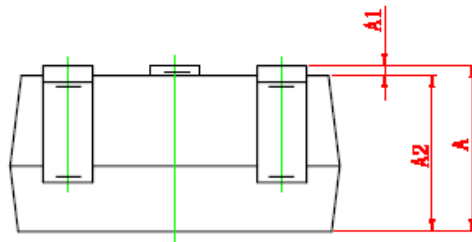
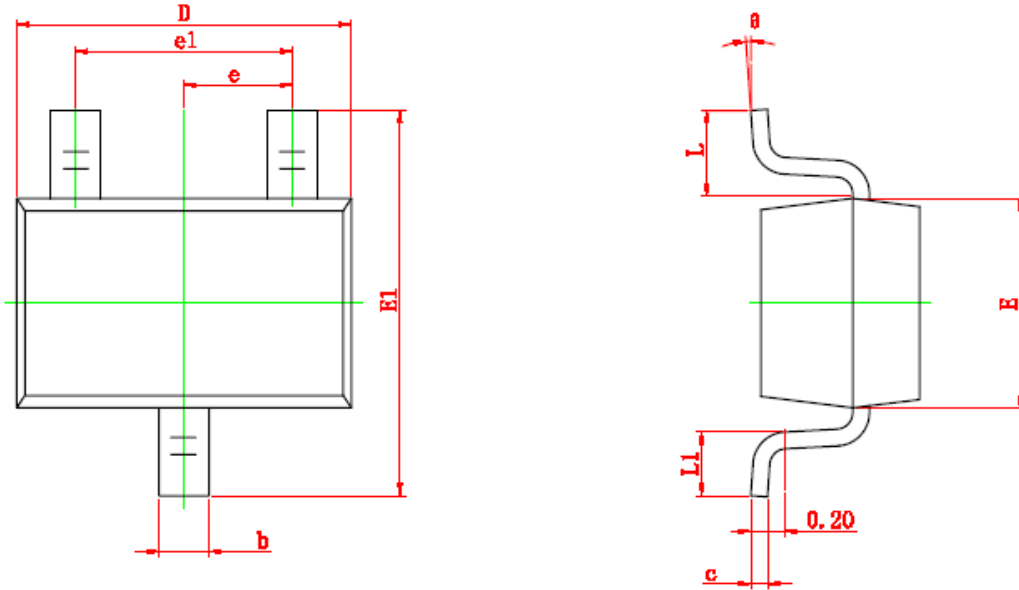




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SOT-323 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°



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