PT4213

Primary Side CC Controller

GENERAL DESCRIPTION

The PT4213 is a primary side regulated constant current controller, which is designed for LED lighting applications. The device is optimized for high performance and cost-effective applications. With Powtech's proprietary constant current compensation technique accurate constant current regulation is achieved without the need of a secondary feedback circuitry. Integrated primary inductance compensation circuitry provides accurate constant current operation despite variations in primary inductance. Excellent EMI performance is achieved with frequency jittering function together with soft driving control at totem pole gate drive output.

The device also features a complete set of protection functions to protect against all fault conditions including output open/short circuit, line under-voltage, and over temperature.

The PT4213 is available in an SOT23-6 package.

FEATURES

- CC without secondary feedback
- Inductance compensation
- Low startup current (<10uA)
- Adjustable primary side current limit
- VCC/FB over voltage protection
- VCC/FB UVLO
- Feedback loop open circuit protection
- Over temperature protection
- RoHS compliant

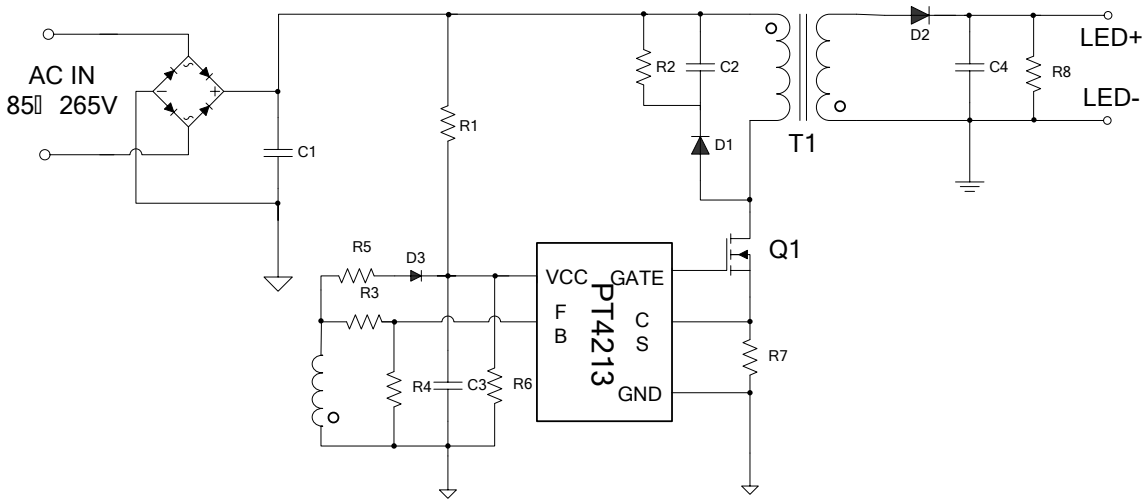
APPLICATIONS

- Off-line High Brightness General LED Lighting
- Integrated LED Lamps such as GU10, E27, PAR20/20/38 LED Lamps

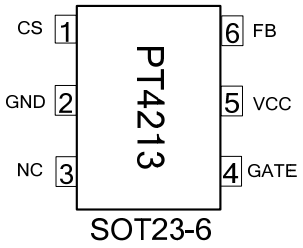
ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
SOT23-6，Pb free	-40℃ to 85℃	PT4213E23F	3000/Tape and Reel	4213

TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



PIN DESCRIPTIONS

PIN No.	PIN NAMES	DESCRIPTION
1	CS	Primary Side Current Sense Input
2	GND	Ground
3	NC	Not connected
4	GATE	Drive output
5	VCC	Power supply, the device is supplied by an auxiliary winding.
6	FB	Auxiliary Winding Voltage Sense Input

ABSOLUTE MAXIMUM RATINGS (note1)

SYM	PARAMETER	VALUE	UNIT
VCC	VCC pin Voltage	-0.3~35	V
V_{FB}	FB pin Input Voltage	-0.3~5	V
V_{CS}	CS pin Voltage	-0.3~5	V
V_{GATE}	GATE pin output voltage	-0.3~15	V
Topt	Operating Junction Temp. Range	-40 to 150	℃
Tstg	Storage Temp. Range	-55 to 150	℃
ESD	HBM	2000	V
RΘJA	SOT23-6	250	℃/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

RECOMMENDED OPERATING RANGE

SYM	PARAMETER	VALUE	UNIT
VCC	VCC pin Operating Voltage	9.5~26	V
T_A	Operating Ambient Temperature	-20~85	℃

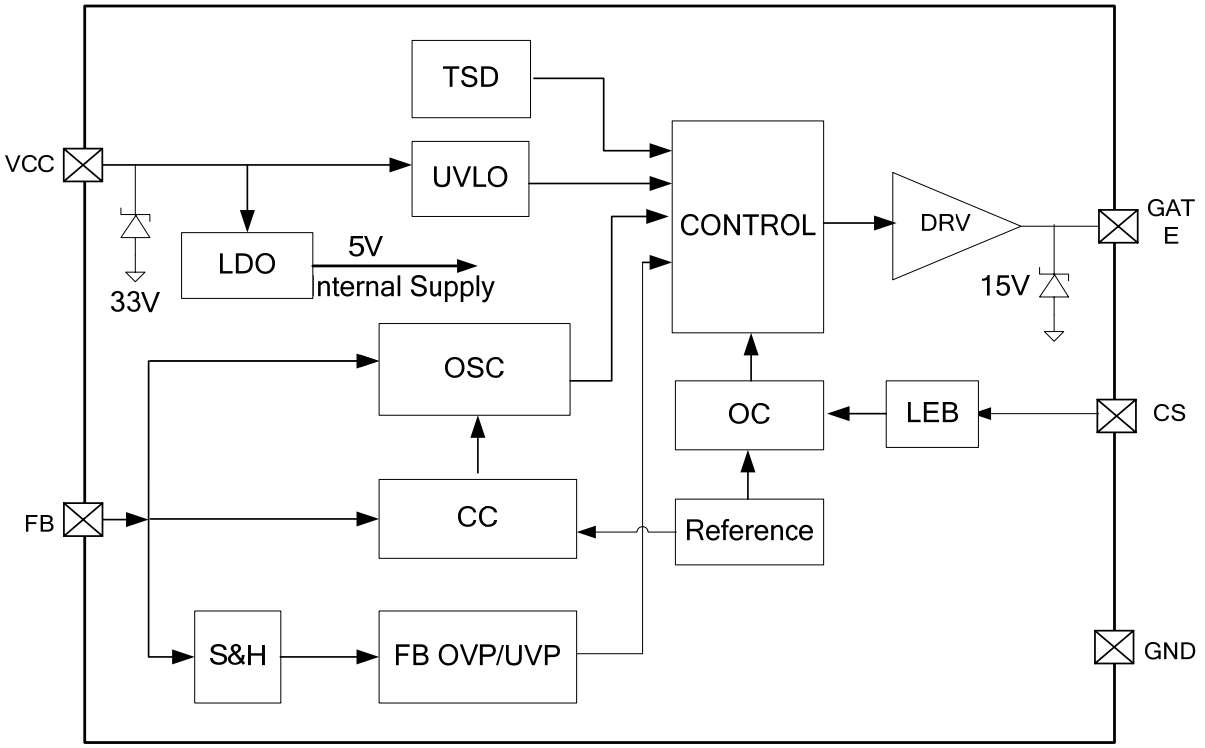
ELECTRICAL CHARACTERISTICS

(T_A=25℃, VCC=16V，f_{sw}=65KHz unless specified otherwise)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

SUPPLY VOLTAGE (VCC)						
I_{START}	Start up current	VCC=13.0V		1	10	uA
V_{VCC_ON}	VCC turn on threshold	VCC Rising	13.5	15.0	16.5	V
V_{VCC_OFF}	VCC minimum operating voltage	VCC Falling	8.0	9.0	10.0	V
V_{VCC_Clamp}	VCC Clamp Voltage	Icc=10mA		33		V
V_{VCC_OVP}	VCC Over Voltage Protection Threshold		26	27.5	29	V
I_{VCCQ}	VCC Supply Current	No switching		350	700	uA
FEED BACK VOLTAGE SENSE PIN (FB)						
V_{FBMAX}	FB Over Voltage Protection		2.4	2.5	2.6	V
V_{FBMIN}	FB Minimum Voltage			0.8		V
I_{FB_OPEN}	FB Open Loop Current			-85		uA
CURRENT SENSE INPUT PIN (CS)						
VCS	Current Limit Threshold	Ifb=0	490	500	510	mV
T_{LEB}	Current sense Leading Edge Blanking Time			250		nS
DRIVE OUTPUT (GATE)						
Dmax	Maximum driving pulse duty cycle			65		%
I_{SOURCE}	GATE Source Current	V_{GS}=12V		200		mA
I_{SINK}	GATE Sink Current	V_{GS}=12V		250		mA
V_{GS_MAX}	Gate clamp voltage			15		V
PROTECTION						
T_{SD}	Thermal Shut Down Threshold			150		℃

SIMPLIFIED BLOCK DIAGRAM



OPERATION DESCRIPTION

The PT4213 consists of an oscillator, feedback circuit, over-temperature protection, frequency jittering, current limit circuit, leading-edge blanking, and constant current control circuitry. The switching frequency is modulated to regulate the output current to provide a constant current characteristic. The PT4213 senses and regulates output current from the primary side of the transformer and is ideal for high precision, high reliability and cost effective LED lighting applications.

THEORY OF OPERATION

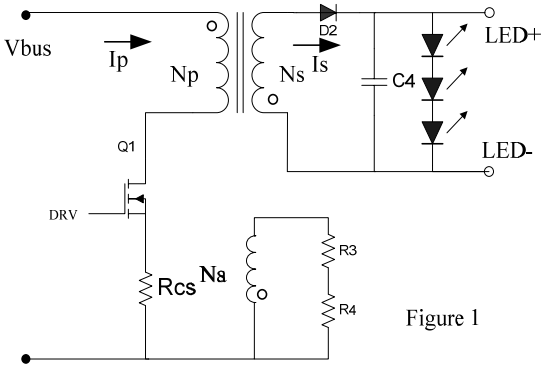


Figure 1

Figure 1 illustrates a simplified flyback converter. When the switch Q1 turns on, the voltage across the primary winding is V_{bus}. Assuming the voltage drop on Q1 is zero, the current in Q1 ramps up linearly at a rate of V_{bus}/L_p. When the current in Q1 reaches a predefined value of I_{pk_pri} , the controller forces Q1 to turn off. During the Q1 on-time, the rectifying diode D2 is reversely biased and the load current Io is supplied by the secondary capacitor C4. When Q1 turns off, D2 conducts and the stored energy is delivered to the output.

The PT4213 is designed to operate in discontinuous conduction mode (DCM). In DCM the energy stored in the primary winding is completely transformed to the secondary winding during each cycle. The output current is determined by R_{cs} and primary/secondary turns ratio of the transformer. Assuming the transformer primary/secondary turns ratio is N_{ps}. The output current is given by following expression:

$$I_{out} = \frac{0.1125}{R_{cs}} * N_{ps}$$

START UP

Once the AC voltage is applied to the application circuit, the V_{bus} charges the V_{CC} pin up through the start

up resistor R1. When the voltage on the V_{CC} pin reaches its V_{CC_ON} threshold, the controller starts to deliver the driving pulses to the power switch Q1 and V_{CC} is then powered by the auxiliary winding. Thanks to the very small start up current, a large start up resistor R1 could be used in the start up circuit to minimize power loss. For the applications with typical 90-264Vac input range, a 1/8W resistor between 0.5Mohm and 3Mohm and a 4.7uF/50V capacitor C3 compose a simple and reliable start up circuit.

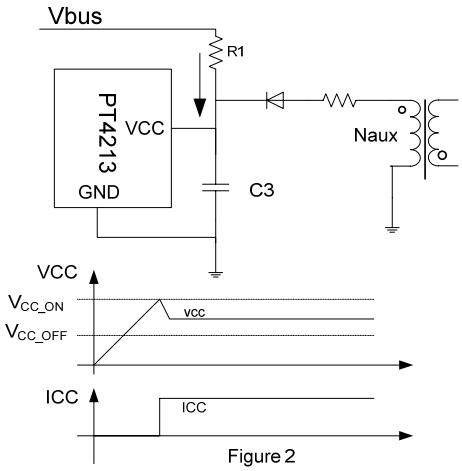


Figure 2

CONSTANT CURRENT (CC) OPERATION

The PT4213 regulates output current using the primary side control. The switching frequency is adjusted as the feedback pin voltage increases to provide a constant output current regulation.

PRIMARY INDUCTANCE COMPENSATION

With the inductance compensation function, the output current is insensitive to primary inductance variation. If the primary magnetizing inductance is either too high or low, the converter will automatically adjust the oscillation frequency to keep the output current constant.

CURRENT SENSE AND LEB

The current of the power MOSFET is converted to a voltage signal through a resistor connected between the source terminal and GND, which is then fed into CS pin. At each switching cycle when the voltage of CS input exceeds an internal threshold, the driving signal is terminated after a short delay. The relationship between the CS threshold and the primary peak current passing through the power MOSFET Q1 follows the following expression:

$$I_{PK\_PRI} = V_{CS} / R_{CS}$$

Where I_{PK_PRI} is the peak current through the power MOSFET, V_{CS} is the voltage threshold of pin1 of the PT4213 and R_{CS} stands for sensing resistor.

A spike is inevitable on the sensed signal on R_{CS} at the moment when the power MOSFET is turned on due to the recovery time of the secondary rectifier and the snubber circuit. The LEB has been implemented in PT4213 to eliminate the effect of the spike. During the LEB time, the current sense comparator is disabled and therefore the switching signal can not be falsely terminated by the turn-on spikes on the sensed signal. With the LEB feature built in, the external RC filter can be removed.

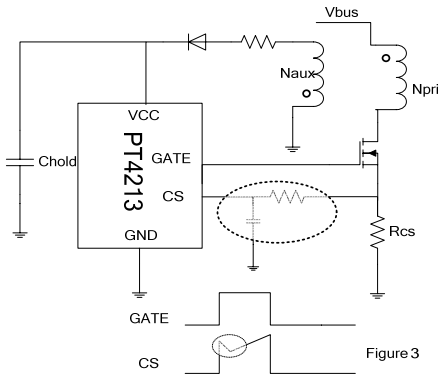


Figure 3

CURRENT LIMIT COMPENSATION

The current limit circuit senses the current in the power MOSFET from the resistor connecting between the source of the power MOSFET and GND. The current sense resistor converts the current in the power MOSFET to a voltage signal, which is then fed to the CS pin. When the voltage at the CS pin exceeds the internal threshold V_{CS} which is set at 500mV, the power MOSFET is turned off for the rest of that cycle. Excellent regulation performance is achieved with Powtech's proprietary line regulation control technique.

SHORT CIRCUIT PROTECTION

In the event of an output short, the PT4213 enters into an appropriate protection mode as described below. When an output short occurs, the feedback pin voltage falls. Once V_{FB} falls below 0.8V during primary winding discharge period, the converter enters into the short circuit

protection mode where the GATE driving is disabled after a delay which is internally set to be around 30 ms. V_{CC} will then drop due to internal power consumption. When V_{CC} drops below the V_{VCC_OFF} turn-off threshold, the PT4213 will be shut down completely. Then the start up sequence will kick in and V_{CC} is charging up again. The device is alternately enabled and disabled till the fault condition is removed.

OPEN CIRCUIT PROTECTION

In the event of output open circuit, the PT4213 enters into an open circuit protection mode as described below. When the output is open circuit, the feedback pin voltage V_{FB} rises. Once V_{FB} is over 2.5 V during the discharge period of the L_p (the inductance of the primary winding of the main transformer), the switching frequency is decreased and the peak current is also decreased to 50%. If the over voltage condition lasts for 8 consecutive cycles, the PT4213 is disabled.

FREQUENCY JITTERING

The frequency jittering is implemented in the PT4213. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

OVER TEMPERATURE PROTECTION

The thermal shutdown circuitry senses the die temperature. When the die temperature is above 150°C the PT4213 is disabled and remains disable until the die temperature falls by 20°C.

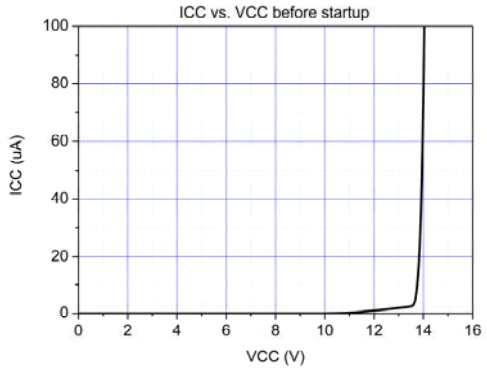
V_{CC} OVER VOLTAGE PROTECTION

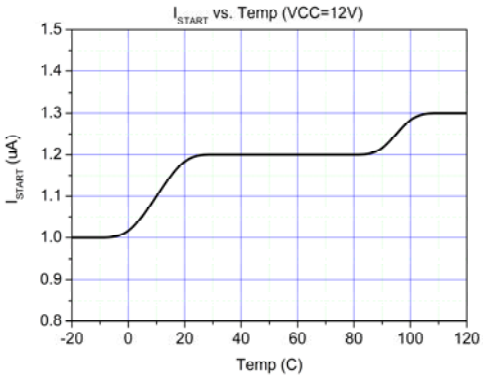
V_{CC} over voltage protection is designed to protect the device from over voltage damage. When the voltage on V_{CC} reaches the OVP threshold, the PT4213 shuts down the GATE driver of the power MOSFET, which causes V_{CC} to drop due to internal power consumption. The PT4213 will recover from OVP status when the voltage on V_{CC} drops below the OVP release threshold.

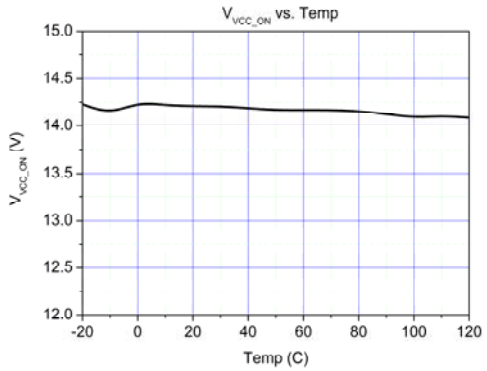
GATE OUTPUT

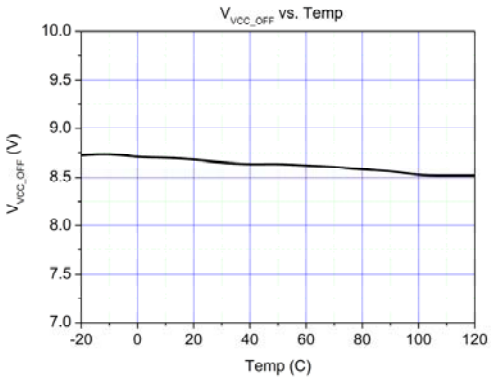
The output drives the GATE of the power MOSFET. The optimized totem-pole type driver offers a good tradeoff between driving capability and EMI. Additionally the output high level is clamped to 15V by an internal clamp to protect the power MOSFET from undesired gate over voltage. A resistor between GATE and GND pulls down the gate voltage to zero at the off state.

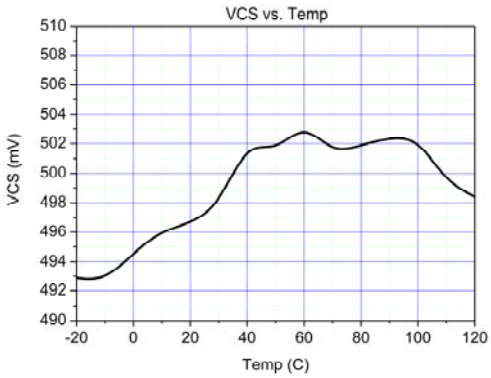
TYPICAL PERFORMANCE CHARACTERISTICS

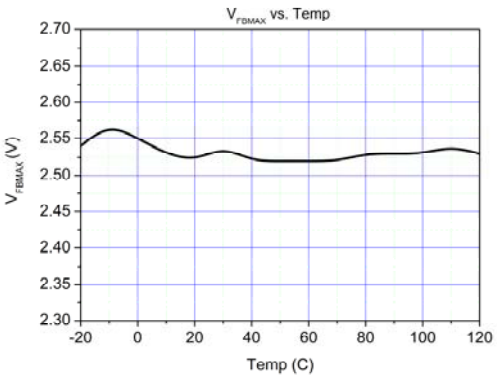












DESIGN Example and Notes:

A design example is given to illustrate step by step how to design a PT4213 based off-line AC/DC LED driver. Refer to figure 4 for the application circuit.

1 Determine input and output

The design spec is given in Table 1. The design objective is to drive 5 x 1W white LEDs in series for general lighting

Table 1

Parameters	Symbol	Limits
Input Voltage	Vin	90-264Vac
Frequency	f_{line}	47-64Hz
Output Voltage	Vout	16V
Max Vout	$Vout_{max}$	17.5V
Min Vout	$Vout_{min}$	15V
Output Current	Iout	320mA

2 Set the switching frequency

The maximum operating frequency is limited by the V_{FB} sampling delay time during the flyback period. To sample FB pin voltage correctly, the secondary side discharge time must be longer than 3.5uS, and then the maximum switching frequency for the PT4213 is limited to 128 KHz. In practice, the appropriate switching frequency for this design is set to be 65KHz considering the EMI, efficiency and the size of the main transformer.

For this design example, the switching frequency f_{sw} and operating period T_{sw} are set as below:

$f_{sw} = 65KHz$

$T_{sw} = 1/f_{sw} = 15.4us$

3 The maximum duty cycle

For the PT4213, the primary winding inductance discharge time t_{dis} is fixed to be 45% of the operating cycle. In order to regulate the LED current precisely, a PT4213 based LED driver should operate in DCM in the entire input voltage range. Therefore,

$$T_{sw} = t_{on} + t_{dis} + t_{dead} \quad (1)$$

t_{on}: turn on time of the switch MOSFET Q1

t_{dis}: discharge time of L_p

t_{dead}: dead time of the flyback DCM mode

$$t_{dis} = 0.45 * T_{sw} \quad (2)$$

$$t_{dead\_min} = 1.5 * 2\pi\sqrt{L_p * C_{ds}} \quad (3)$$

For this design example, the minimum t_{dead_min} can be estimated to be approximately 20% of the switch cycle as a start point and then adjusted after the LED driver is implemented.

$$t_{dead\_min} = 1.5 * 2\pi\sqrt{L_p * C_{ds}} = 20\% * T_{sw} = 3.08us$$

$$t_{dis} = 45\% * T_{sw} = 6.93us$$

$$t_{on\_max} = T_{sw} - t_{dis} - t_{dead\_min}$$

$$D_{max} = t_{on\_max} / T_{sw} = 35\%$$

4 Turns Ratio

The maximum allowable N_{ps} is determined by the voltage stress on the power switch Q1, the minimum operating voltage $V_{in\_dc\_min}$ and the primary side inductance L_p. The minimum allowable N_{ps} is limited by the maximum allowable reverse voltage on the secondary rectifying diode D3. Therefore the selection of N_{ps} is a trade-off among the following factors: Drain-Source breakdown voltage of the power switch Q1, the breakdown voltage of the secondary rectifying diode D3, the primary side inductance L_p, the primary peak current I_{pk_pri}, and the minimum operating input voltage $V_{in\_dc\_min}$. The smaller the N_{ps}, the smaller the $V_{in\_dc\_min}$, and the less bulk capacitance is required. However, a small N_{ps} will need higher reverse voltage for the secondary rectifying diode D3. In practice, the recommended N_{ps} is less than 5.0 for general applications with 85VAC-265VAC input.

$$V_{in\_dc\_min} * t_{on\_max} = N_{ps} * V_{out} * t_{dis} \quad (4)$$

From equation (4), the following equation can be derived as:

$$N_{ps} = V_{in\_dc\_min} * t_{on\_max} / V_{out} * t_{dis} \quad (5)$$

In this design example, the minimum operating input voltage is estimated to be approximately 60Vdc as a start point.

$$N_{ps} = V_{in\_dc\_min} * t_{on\_max} / V_{out} * t_{dis} = 60 * 5.39 / 16 * 6.93 = 2.92$$

5 Calculate the current sense resistor

Once N_{ps} is determined, the current sense resistor R_{cs} can be calculated from the following expressions:

$$R_{cs} = \frac{0.1125}{I_{out}} * N_{ps} \quad (6)$$

$$I_{pk\_pri} = \frac{V_{cs}}{R_{cs}} = \frac{0.5V}{R_{cs}} \quad (7)$$

For this design example,

$$R_4 = R_{cs} = \frac{0.1125}{I_{out}} * N_{ps} = \frac{0.1125 * 2.92}{0.32} = 1.0\Omega$$

$$I_{pk\_pri} = \frac{V_{cs}}{R_{cs}} = \frac{0.5V}{R_{cs}} = \frac{0.5V}{1.0\Omega} = 0.5A$$

6 Calculate the primary inductance

Primary inductance L_p is determined by the output power, the switching frequency f_{sw}, the primary peak current I_{pk_pri} and the flyback converter efficiency η.

The relationship between the primary and secondary energy is given by:

$$\frac{1}{2} L_p * I_{pk-pri}^{\ 2} * F_{sw} * \eta = V_{out} * I_{out} \quad (8)$$

From the equation (8), the primary inductance L_p of the main transformer can be derived as:

$$L_p = \frac{2 * V_{out} * I_{out}}{I_{pk-pri}^{\ 2} * F_{sw} * \eta} \quad (9)$$

For this design example,

$$L_p \le \frac{2 * V_{out} * I_{out}}{I_{pk-pri}^{\ 2} * F_{sw} * \eta} = \frac{2 * 16 * 0.32}{0.5^2 * 65 * 10^3 * 0.90} = 0.7mH$$

For this design example, L_p is chosen to be 660uH.

7 Calculate the primary winding

In order to keep the transformer from saturation, the maximum flux density must not be exceeded. Therefore the minimum primary winding turns must meet the following criteria:

$$N_p = \frac{L_p * I_{pk\_Pri}}{A_e * \Delta B_{max}} \quad (10)$$

Where ΔB_{max} is the maximum allowed flux density and Ae is the core effective area.

For this design example, EE16 core is selected. From the EE16 transformer core datasheet, Ae is 19.2,

ΔB_{max} is chosen to be 2500 Gauss.

Then,

$$N_p = \frac{L_p * I_{pk\_pri}}{A_e * \Delta B_{max}} = \frac{0.66 * 10^{-3} * 0.5}{19.2 * 10^{-6} * 0.25} = 68.75$$

69 turns is chosen for this deign example.

8 Calculate the secondary winding

The secondary winding turns can be calculated:

$$N_s = \frac{N_p}{N_{ps}} \quad (11)$$

For this design example,

$$N_s = \frac{N_p}{N_{ps}} = \frac{69}{2.92} = 23.63$$

23 turns is chosen for this design example.

9 Calculate the auxiliary winding

The auxiliary winding turns can be calculated:

$$N_a = \frac{V_{cc}}{V_{out}} * N_s \quad (12)$$

In practice Vcc is set to be 12V.

For this design example,

$$N_a = \frac{V_{cc}}{V_{out}} * N_s = \frac{12}{16} * 23 = 17.25$$

17 turns is chosen for this design example.

10 Determine feedback resistors R_{fb_up} and R_{fb_dn}

For optimum regulation, the current flowing out of FB pin of the PT4213 at 220VAC input voltage should be approximately 1mA. Therefore the R_{fb_up} is given by:

$$R_{fb\_up} = \frac{\sqrt{2} * 220V}{1mA} * \frac{N_a}{N_p} \quad (13)$$

R_{fb_up} unit is $K\Omega$.

For this design example,

$$R_5 = R_{fb\_up} = \frac{\sqrt{2} * 220V}{1mA} * \frac{17}{69} = 76.6K\Omega$$

R5 is chosen to be $75K\Omega$ for this design.

The low side feedback resistor is selected to set the output OVP. R_{fb_dn} should be selected so that when the output voltage reaches OVP, the voltage on FB pin reaches V_{FBMAX} during transformer reset time. The relationship between V_{ovp} and V_{FBMAX} is:

$$V_{FBMAX} = \frac{R_{fb\_dn}}{R_{fb\_up} + R_{fb\_dn}} \frac{N_a}{N_s}\left(V_{ovp} + V_d\right) \quad (14)$$

Re-arrange above expression R_{fb_dn} can be derived as:

$$R_{fb\_dn} = \frac{V_{FBMAX} * R_{fb\_up}}{\frac{N_a}{N_s}\left(V_{ovp} + V_d\right) - V_{FBMAX}} \quad (15)$$

V_d: forward voltage drop of the secondary side rectifier diode, V_{FBMAX} is maximum FB pin operating voltage which has a typical value of 2.5V.

For this design example,

$$R_6 = R_{fb\_dn} = \frac{2.5 * 75}{\frac{17}{23}(20 + 0.5) - 2.5} = 14.82K\Omega \cdot$$

R6 is chosen to be 15 $K\Omega$; output OVP is set to be 20V for this design example.

11 Select the secondary and auxiliary rectifying diode

Maximum reverse voltage on secondary and auxiliary rectifying diode is:

$$V_{sec\_diode} \geq \left(\frac{\sqrt{2} * 265 * N_s}{N_p} + V_{out}\right) \quad (15)$$

$$V_{aux\_diode} \geq \left(\frac{\sqrt{2} * 265 * N_a}{N_p} + V_{cc}\right) \quad (16)$$

Peak current flowing in secondary rectifying diode is:

$$I_{pk\_sec} = 0.5 * N_{ps} \Big/ R_{cs} \quad (17)$$

The secondary rectifying diode should be selected with the break down voltage higher than V_{sec_diode} and average forward current should be selected based on the output current and the secondary peak current. The auxiliary rectifying diode should be selected with the break down voltage higher than V_{aux_diode}.

12 PCB Layout

The circuit shown in Figure 4 is configured as a primary-side regulated off-line flyback power supply utilizing PT4213 with 320mA CC output for driving 5x 1W LED in series.

AC input power is rectified by BD1. The rectified DC is filtered by the bulk capacitors C1 and C2. Inductor L1, C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI noise.

The secondary side of the transformer is rectified by D3. An ultra fast recovery diode and filtered by C5.

The feedback resistors (R5 and R6) with standard 1% tolerance should be selected for closed LED current. The feedback resistors should be placed as close to the FB pin as possible to minimize noise.

R1, R2 and C4 form the start up circuit. The auxiliary winding provides power to the PT4213 through R7 and D2. C4 should be place as close as possible to the VCC and GND pins.

R4 is the primary side current sense resistor, which should be placed close to the CS pin of the PT4213.

REFERENCE CIRCUIT FOR DRIVING 5X1W LED

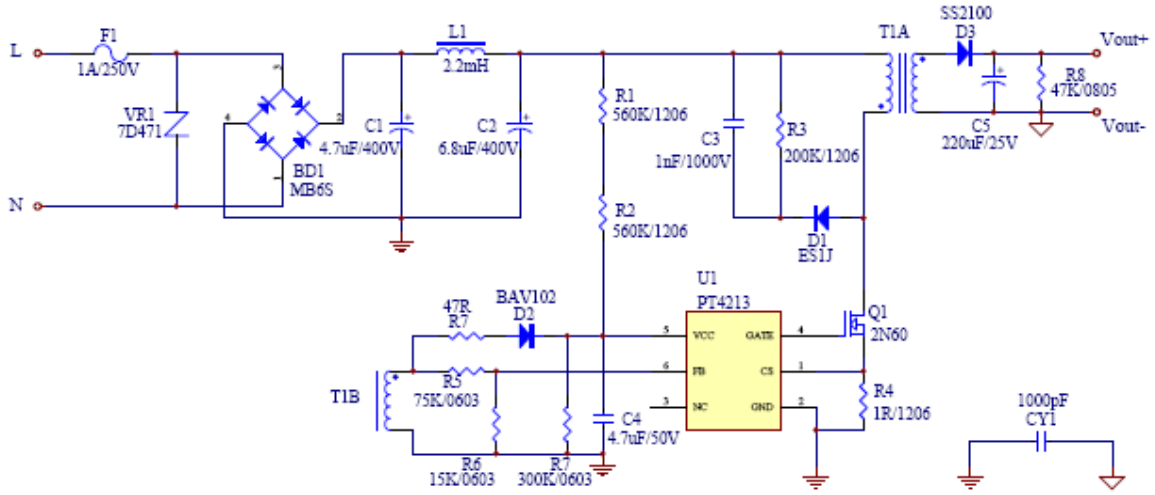
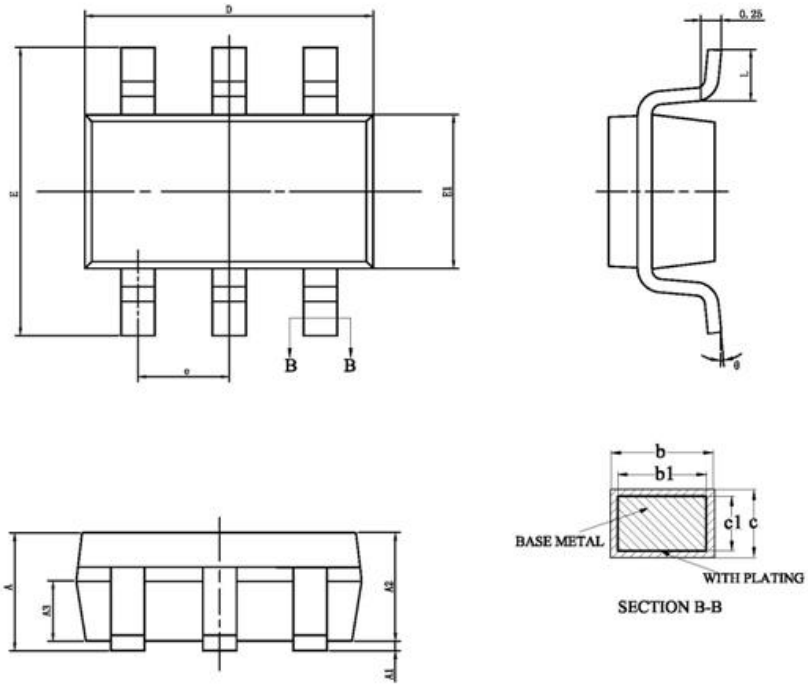


Figure 4

PACKAGE INFORMATION

SOT23-6



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.30
A1	0.04	0.07	0.10
A2	1.00	1.10	1.20
A3	0.55	0.65	0.75
b	0.34	—	0.43
b1	0.33	0.35	0.38
c	0.15	—	0.21
c1	0.14	0.15	0.16
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95BSC		
L	0.30	—	0.60
θ	0	—	8°