18V/2A High Efficiency Synchronous Rectified Step -Down DC/DC Converter

❖ GENERAL DESCRIPTION

The MA5201 is a high efficiency synchronous step-down DC/DC converter series with 2A continuous output current supplied.

A built-in Under Voltage Lockout (UVLO) circuit is provided to prevent start-up until the input voltage reaches to 4.6V. In addition, it features over-current protection and thermal shutdown. To improve the light load efficiency, it is designed as the power saving mode (PSM) to minimize the switching loss by reducing the switching frequency.

The MA5201 is available in SOT23_6L package.

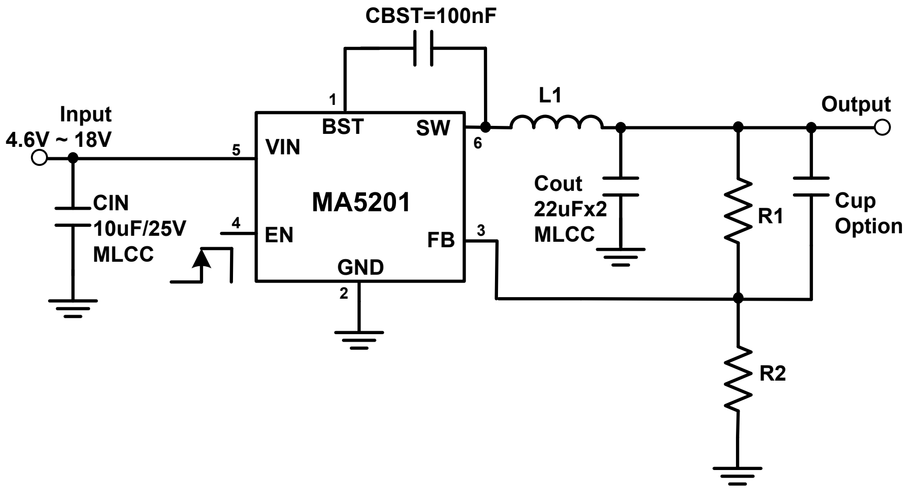
❖ FEATURES

- Wide 4.6V to 18V Operating Input Range
- Integrated 120/80mΩ Power MOSFET Switches
- Adjustable Output Voltage from 0.6V to 12V
- Power Saving Mode (PSM) during the light Load Operation
- High Efficiency up to 95%
- Adjustable Output Voltage from 0.6V to 12V
- 2A Continuous Output Current
- 500kHz Constant Frequency Operation
- Current Mode Operation
- Over-temperature and Over-current Protection
- Input Under Voltage Lockout (UVLO)
- 10μA Shutdown Current
- RoHS Compliant (100% Green Available)

❖ APPLICATIONS

- Data comm. DSL CPE Graphics Cards
- Set-Top-Box, DVD
- Servers/Networking
- Telecomm Equipment
- LCD Monitor and LCD TV

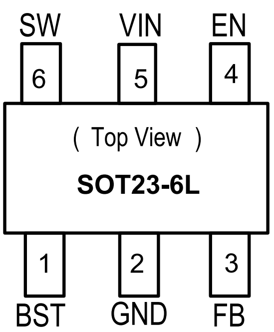
❖ APPLICATION CIRCUIT



$V_{OUT}=V_{FB}\times(1+R1/R2)$, $V_{FB}=0.6V$,

❖ PIN ASSIGNMENT

The package of MA5201 is SOT23-6L; the pin assignment is given by:

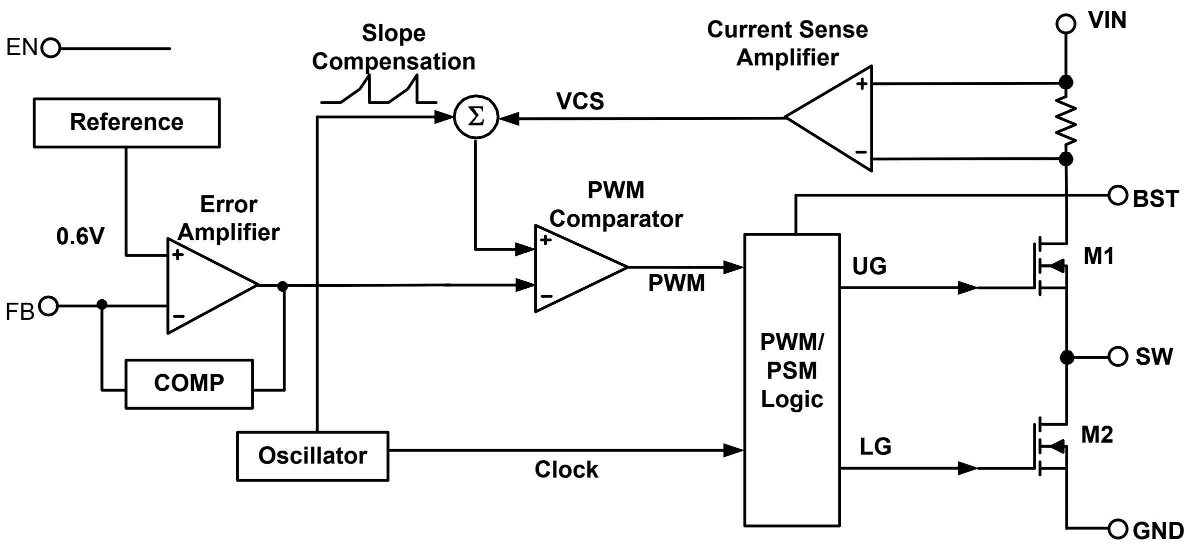


Name	Description
BST	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
GND	Ground Pin.
FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: Vout=0.6*(1+R1/R2)
EN	Enable control. Pull high to turn on. Do not float.
VIN	Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap
SW	Inductor pin. Connect this pin to the switching node of inductor

❖ RDER/MARKING INFORMATION

Order Information	Top Marking
MA5201 X X Package Type C: SOT23-6L Packing Blank : Bag A : Taping	D1 Y WX ID Code: Internal Week: 01~26(A~Z) 27~52(a~z) Year : 6 = 2016

❖ BLOCK DIAGRAM



❖ ABSOLUTE MAXIMUM RATINGS (Note1,at T_A=25°C)

Characteristics	Symbol	Rating	Unit
Supply Voltage	V_{IN}	21	V
Switch Node Voltage	V_{SW}	–1 to V_{IN} +0.3	V
EN Voltage	V_{EN}	–0.3to V_{IN} +0.3	V
Boost Voltage	V_{BS}	V_{SW} + 6	
All Other Pins		–0.3 to +6	V
Lead Temperature		260	°C
Storage Temperature		–65 to +150	°C
Junction Temperature	T_J	–40 to 150	°C
Thermal information (Note 3,4)			
Maximum Power Dissipation	PD	0.8	W
Thermal Resistance from Junction to case	θ_{JC}	66	°C/W
Thermal Resistance from Junction to ambient	θ_{JA}	125	°C/W

Characteristics	Symbol	Rating	Unit
Recommend Operating Conditions (Note2)			
Input Voltage	V_{IN}	+4.6 to 18	V
Operation Temperature	T_{OT}	–40 to +85	°C
Junction Temperature	T_{OJ}	–40 to 135	°C

Note (1): Stress exceeding those listed “Absolute Maximum Ratings” may damage the device.
Note (2): The device is not guaranteed to function outside of the recommended operating conditions.
Note (3): Measured on JESD51-7, 4-Layer PCB.
Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature TJ_MAX, the junction to ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD_MAX= (TJ_MAX-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

❖ ELECTRICAL CHARACTERISTICS

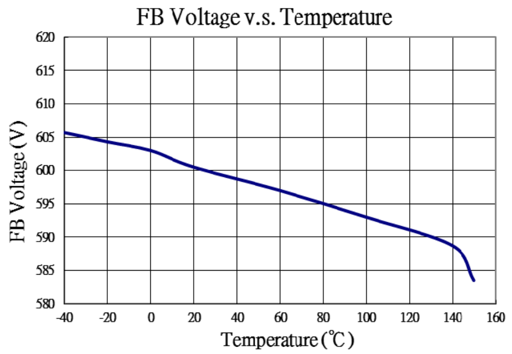
(V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

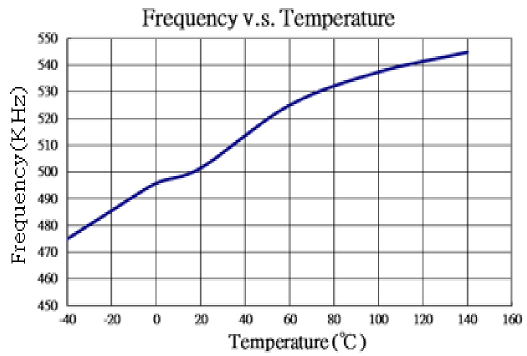
Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		10		μA
Regulated Feedback Voltage	V_{FB}	4.6V ≦ V_{IN} ≦ 18V	0.584	0.6	0.616	V
Current Limit		Vo=1V		3.5		A
SW Leakage Current		V_{EN} = 0V, V_{SW} = 0V			10	μA
High Side On Resistance	$HR_{DS(ON)1}$			0.12		Ω
Low Side On Resistance	$LR_{DS(ON)1}$			0.08		Ω
Oscillation Frequency	F_{OSC}		400	500	600	kHz
Short Circuit Oscillation Frequency	F_{SCP}	V_{FB}=0V		167		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.5V		90		%
Minimum Duty Cycle	D_{MIN}	V_{FB}=1.2V			0	%
Minimum On Time	$T_{ON(min)}$			100		ns
Under Voltage Lockout Threshold	UVLO	V_{IN} Rising	3.85	4.3	4.58	V
Under Voltage Lockout Threshold Hysteresis	UVLO-Hys			350		mV
Thermal Shutdown Threshold	T_{SD}			155		℃
EN High Level	V_{EN}		2.80			V
EN Low Level					0.6	V
EN Input Current		V_{EN} = 1V		14		μA

Note: Guaranteed by design.

❖ TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, C_{IN}=10μF, C_{OUT}=22μFx2, T_A=+25℃

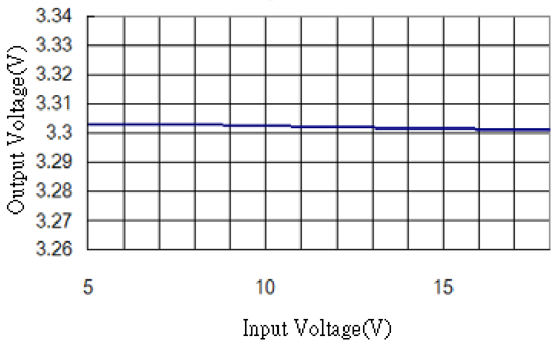




Line Regulation

V_{IN}=5V~18V, V_{OUT}=3.3V, Io=0.5A

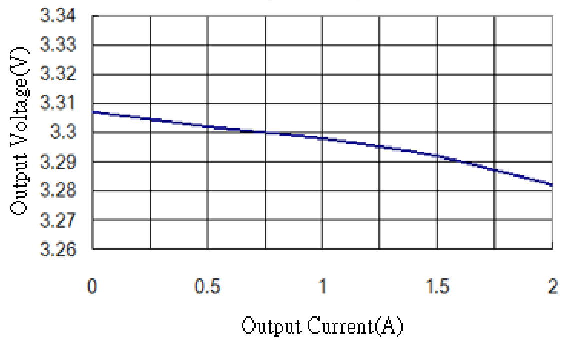
Output Voltage VS. Input Voltage



Load Regulation

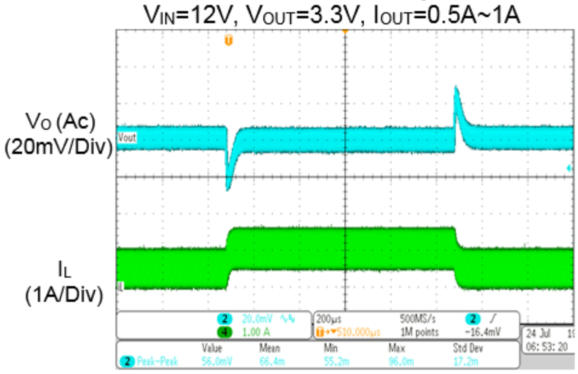
V_{IN}=12V, V_{OUT}=3.3V, Io=0A~2A

Output Voltage VS. Output Current



Load Transient Response

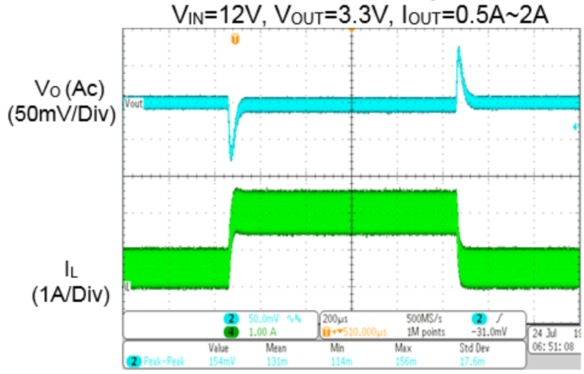
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.5A~1A



Time: (200uS/Div)

Load Transient Response

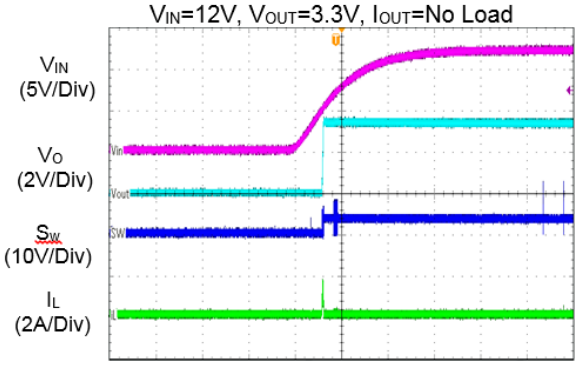
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.5A~2A



Time: (200uS/Div)

Power ON

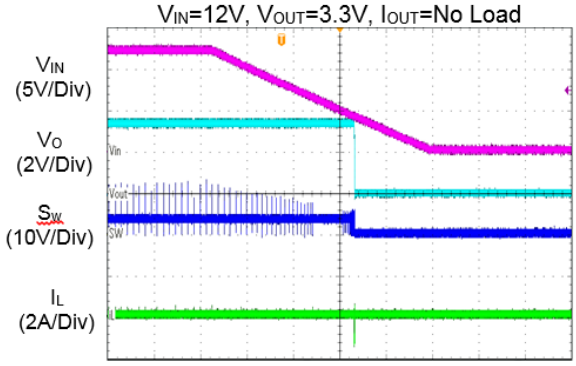
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=No Load



Time: (4mS/Div)

Power Off

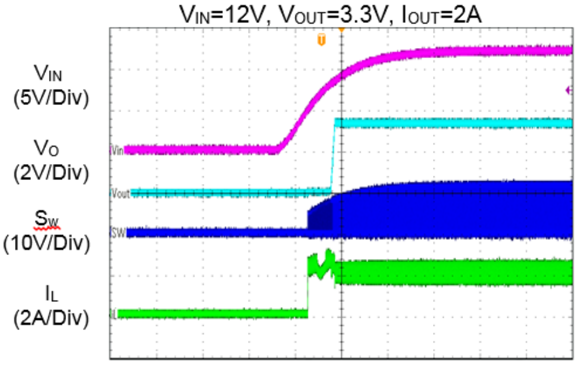
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=No Load



Time: (20mS/Div)

Power ON

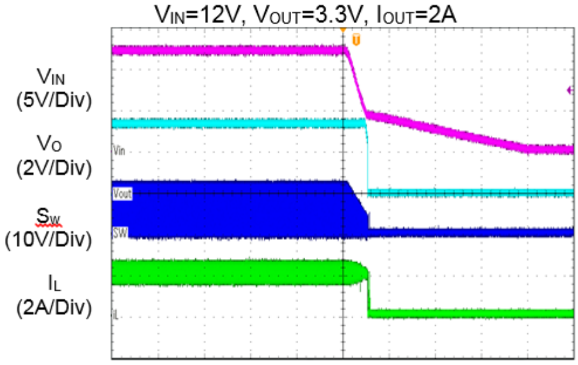
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A



Time: (4mS/Div)

Power Off

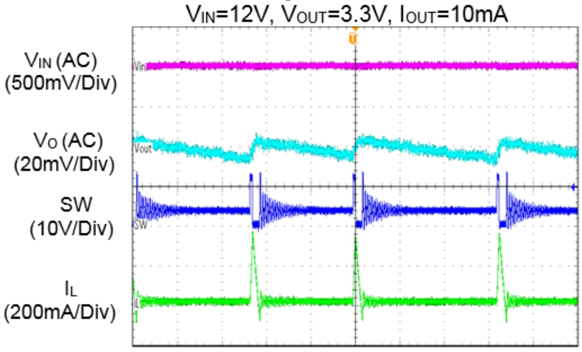
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A



Time: (10mS/Div)

Steady State Waveforms

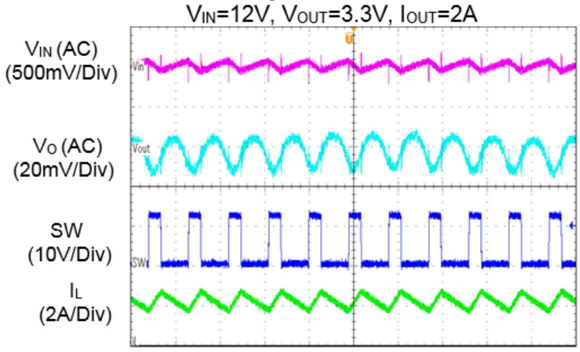
V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA



Time: (4uS/Div)

Steady State Waveforms

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A



Time: (2uS/Div)

Detailed Description

The MA5201 is a current mode PWM synchronous step-down converter with a constant switching frequency. It regulates the input voltage from 4.6V to 18V and a low output voltage of 0.6V.The supplied load current is up to 2A.

Power Saving Mode

The switching losses resulted from the Miller capacitance of the MOSFET are the dominant power dissipation parameters at light load. The power saving mode at light load can minimize the switching loss by reducing the switching frequency. Therefore, the MA5201 is designed as the power saving mode for high efficiency at light load.

Oscillator Frequency

Slope compensated current mode PWM control provides not only stable switching and cycle-by-cycle current limit for superior load and line response but also protection of the internal main switch and synchronous rectifier. The MA5201 switches at a constant frequency (500 kHz) and regulates the output voltage. The PWM comparator modulates the power transferred to the load by changing the inductor's peak current based on the feedback error voltage during each cycle. The main switch is turned on for a certain period to ramp the inductor's current at each rising edge of the internal oscillator under normal operation whereas off when the inductor's peak current is above the error voltage. After the main switch is turned off, the low side MOS will be turned on immediately and stay on until the next cycle starts.

Short Circuit Protection

The MA5201 provides short circuit protection. When the output is shorted to ground, the oscillator's frequency is reduced to prevent the inductor's current from increasing beyond the NMOS current limit. The NMOS current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

Maximum Load current

The MA5201 can operate down to 4.6V input voltage; however the maximum load current decreases at lower input due to large IR voltage drop on the main switch and low side switch. The slope compensation signal reduces the inductor's peak current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Enable

The EN pin provides electrical on/off control of the regulator. Once the voltage of the EN pin exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the voltage of the EN pin is pulled below the threshold, the regulator will stop switching and the internal slow start reset. If the EN pin is open, it will be pulled to low by the internal circuit.

Under Voltage Lockout

The MA5201 incorporates an under voltage lockout circuit to keep the device disabled when VIN is below the UVLO start threshold. During power-up, the internal circuit is held inactive until VIN exceeds the UVLO start threshold voltage. Once this threshold voltage is reached, device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteretic in the UVLO comparator is 350mV.

Boost Capacitor

The BST pin and SW pin can be connected by a 100nF low ESR ceramic capacitor, providing the gate drive voltage for the high side MOSFET.

Thermal Shutdown

The MA5201 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold, the voltage reference will be grounded and high side MOSFET turned off.

Application Information

Input Capacitor Selection

It is necessary for the input capacitor to sustain the ripple current produced during the period of “on” state of the upper MOSFET, so a low ESR is required to minimize the loss. The RMS value of this ripple can be obtained by the following:

$$I_{INRMS} = I_{OUT}\sqrt{D \times (1 - D)}$$

Where D is the duty cycle, I_{INRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. The loss of the input capacitor can be calculated by the following equation:

$$P_{CIN} = ESR_{CIN} \times I_{INRMS}{}^{2}$$

Where P_{CIN} is the power loss of the input capacitor and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large di/dt through the input capacitor, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge-protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor selection is to meet the requirements of the output voltage ripple and affects the load transient response. The higher inductance can reduce the inductor's ripple current and induce the lower output ripple voltage. The ripple voltage and current can be approximately calculated approximated by the following equations:

$$\Delta I = \frac{V_{in} - V_{out}}{F_S \times L} \bullet \frac{V_{out}}{Vin}$$

$$\Delta V_{out} = \Delta I \times ESR$$

Although the increase of the inductance reduces the ripple current and voltage, it contributes to the decrease of the response time for the regulator to load transient as well. Increasing the switching frequency (Fs) for a given inductor also can reduce the ripple current and voltage but it will increase the switching loss of the power MOS.

The way to set a proper inductor value is to have the ripple current (△I) be approximately 10%~50% of the maximum output current. Once the value has been determined, select an inductor capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) is reasonable tolerance able to be met by most manufacturers. For some types of inductors, especially those with core made of ferrite, the ripple current will increase abruptly when it saturates, resulting in a larger output ripple voltage.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. The high capacitor value and low ESR will reduce the output ripple and the load transient drop. These requirements can be met by a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number Of Capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

ΔV_{ESR} = change in output voltage due to ESR
$\Delta IOUT$ = load transient.
ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).
ESR_{MAX} = maximum allowable ESR.
High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. For the decoupling requirements, please consult the capacitor manufacturers for confirmation.

Output Voltage

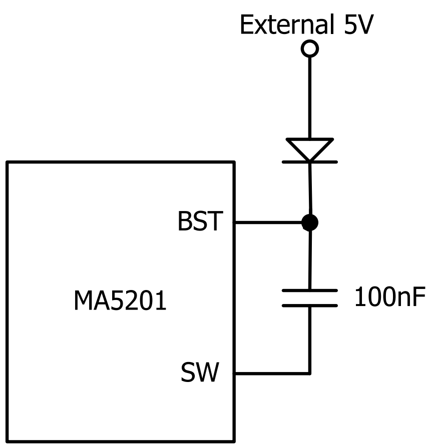
The output voltage is set using the FB pin and a T-type resistor connected to the output as the circuit shown below.

The output voltage (V_{out}) can be calculated according to the voltage of the FB pin (V_{FB}) and ratio of the feedback resistors by the following equation, where (V_{FB}) is 0.6V:

$$V_{out} = 0.6 \times \frac{(R_1 + R_2)}{R_2}$$

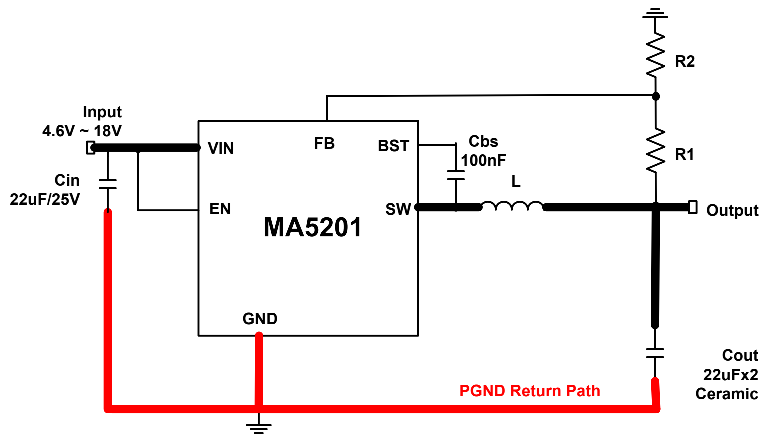
External Bootstrap Diode

When the condition Duty Cycle > 65% occurs, it is strongly recommended to add an external bootstrap diode (such as IN4148 or BAT54) between an external 5V and BST pin for efficiency improvement. The external 5V should be lower than 5.5V.



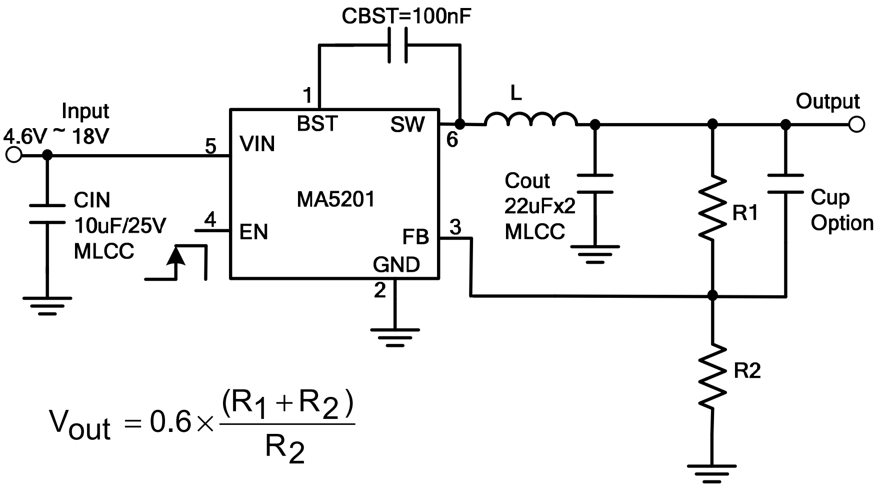
Layout Consideration

For proper operation of the converter, some layout rules should be followed. It is necessary to understand which pin of MA5201 is sensitive and which is insensitive. Please refer the following for the location where noise comes from on the circuit and where the clear ground is for the small signal ground.



1.) First, put the input capacitor (C_{IN}) as close as possible to the VIN pin.
2.) Secondly, place the Cs, Rs, Cp, Css and R2 as close as MA5201 and connect these analog grounds (Clear AGND) to MA5201's GND pin. It is recommended to use a dot short for these AGND pins or connect the GND pin via contact.
3.) The large current loop shown in bold lines in the above figure circuit should be routed as short and wide as possible and the switch node is a high dv/dt. It easily couples noise to other traces by the capacitive path. Therefore the sensitive signals like FB, COMP and AGND should be routed away with this noise source.
4.) The feedback network resistors (R1 & R2) should be routed away from the inductor and switch node to minimize noise and EMI issue. And the R1 resistor should be sensed the output capacitor or device loading, not the inductor's output node.

Application 1: (Typical)



$$V_{out} = 0.6 \times \frac{(R_1 + R_2)}{R_2}$$

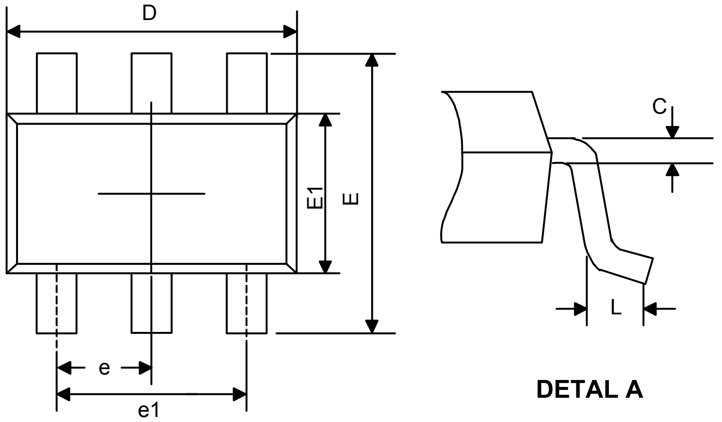
(Recommended component values)

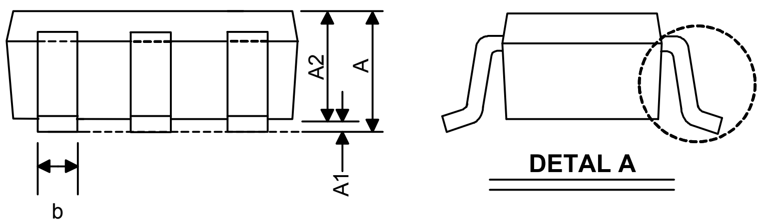
Application 1 (Typical)				
Vout (V)	L (uH)	R1 (KΩ)	R2 (KΩ)	Remark
1	4.7	86.6 (1%)	130 (1%)	
1.2	4.7	86.6 (1%)	86.6 (1%)	
1.5	4.7	86.6 (1%)	57.6 (1%)	
1.8	4.7	86.6 (1%)	43.2 (1%)	
2.5	6.8	86.6 (1%)	27.4 (1%)	
3.3	6.8	86.6 (1%)	19.1 (1%)	
5	6.8	86.6 (1%)	11.8 (1%)	

Use 1% Resistor

Qty	Ref	Value	Description	Package
2	Cout	22μF	Ceramic Capacitor X5R 16V Murata-part number: GRM32ER61C226KE20L	1206
1	CIN	10uF	Ceramic Capacitor X5R 25V	1206
1	CBST	100nF	Ceramic Capacitor	0603
1	L	4.7u~6.8uH	Inductor, Rated Current 3.5A TDK:APM6530T WE:74477 CYNTEC:PCMB104T	SMD
1	U1	MA5201	Step-Down DC/DC Converter	SOT23_6L

❖ PACKAGE OUTLINES





Symbol	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.00	-	1.45	0.039	-	0.057
A1	0.05	-	0.15	0.002	-	0.085
A2	0.90	1.10	1.30	0.035	0.043	0.051
b	0.30	-	0.50	0.012	-	0.020
C	0.08	-	0.22	0.003	-	0.009
D	2.70	2.90	3.10	0.106	1.114	0.122
E1	1.40	1.60	1.80	0.055	0.063	0.071
E	2.60	2.80	3.00	0.102	0.110	0.118
L	0.30	-	0.60	0.012	-	0.024
e1	1.80	1.90	2.00	0.071	0.075	0.079
e	0.85	1.00	1.15	0.033	0.037	0.045