APPLICATION INFORMATION

Predictive Timing Operation

The essence of SP6002 is the predictive timing circuitry that is based on several U.S. patented technologies. This assures higher rectification efficiency by a) eliminating high cross conduction current under all operating conditions and b) significantly reducing the body diode conduction losses in the synchronous rectifier.

VDD Decoupling Capacitor

The IC is sensitive to large supply voltage ripple. If the IC drives a MOSFET with significant input capacitance, Ciss, the ripple due to gate drive energy transfer can create large ripple. Therefore, it is most suitable to add a high frequency decoupling ceramic capacitor of 0.01μF~0.1μF between Vdd to ground, and the capacitor should be placed as close proximity to the driver as possible.

Adjusting ON Delay

The ON delay control imposes a minimum time after the Catch MOSFET gate was turned off before the Forward MOSFET gate is turn on. This is particularly important for operation during discontinuous current operation. The figure 1 below shows the ON delay function during normal operation. The Forward MOSFET gate voltage turns on at the falling edge of the Catch gate voltage, Vgs.

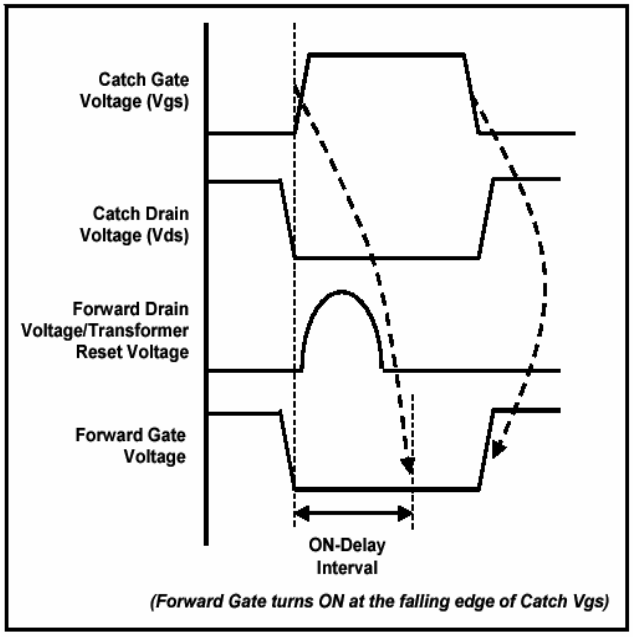


Fig. 1

The next figure shows the ON delay function during light load or start-up. The Forward MOSFET gate voltage turns on after the ON-Delay interval is completed.

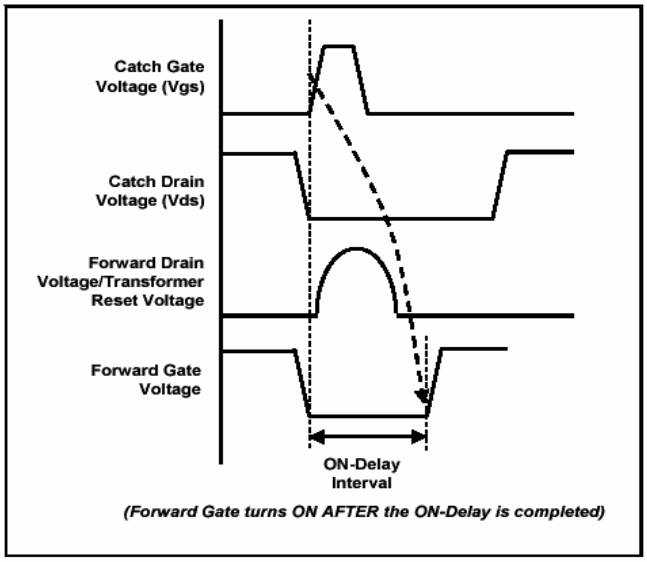


Fig.2

The ON delay is adjusted by the value of capacitance connected from GND to ON Delay pin on the SP6002. The required capacitor value is highly dependent on the transformer-reset method. Forward converters can be reset by 1) diode method, 2) passive RC method, or 3) active method. The suggested starting value for the ON Delay Capacitor is like as Fig3..

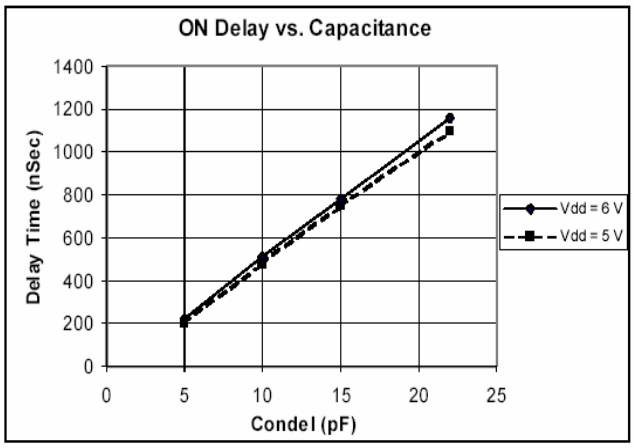


Fig.3

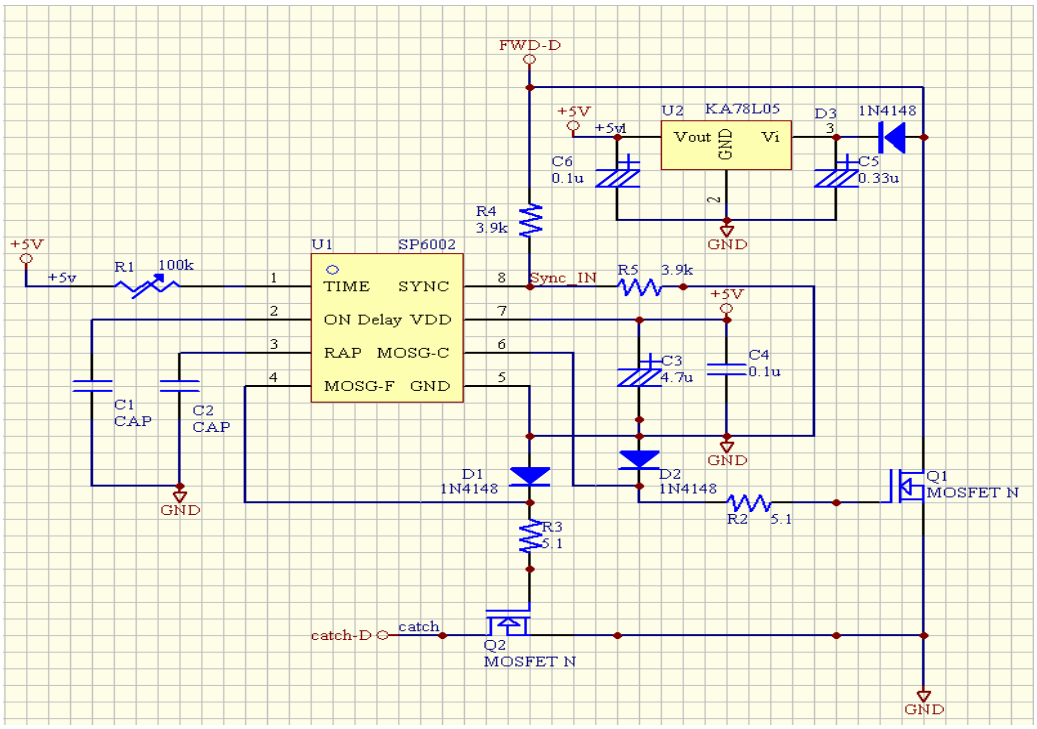


Fig. 4 Application Schematic

Timing Adjustment

The Timing pin provides adjustment of the patented dv/dt filter circuit that differentiates between the real power and ring-back no-power transformer secondary voltage positive waveform. Under light or no load conditions, the output current will be discontinuous. For that condition the transformer voltage "rings" back positive. The SP6002 detects positive transformer secondary voltage to establish power transmission, and determines the SR MOSFET turn ON time. However, it is not desirable to turn on the MOSFET during the "ring-back". The dv/dt filter detects the true power pulse from the "ring-back".

The Timing adjustment should be performed under heavy load circumstance. A variable resistor, 0~100KΩ, is connected from Timing pin to V_{DD} and adjust the variable resistor. Changing the resistor value will change dv/dt slope. This resistor value normally is from 8Kohm to 20Kohm. The typical relation between resistor value and the Delta T is shown in Fig.5.

Once the resistor value is adjusted correctly, the SP6002 gate will be triggered as shown in Fig.6 & Fig.7 .

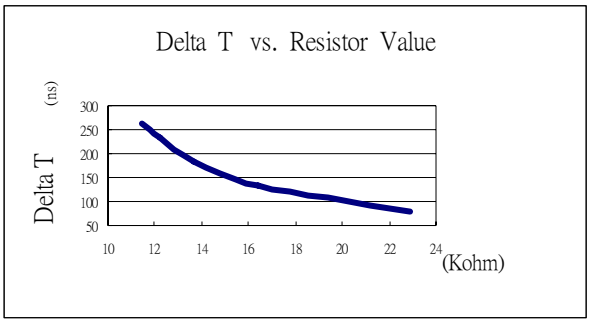


Fig.5 R_{Timing} **v.s** Delta T

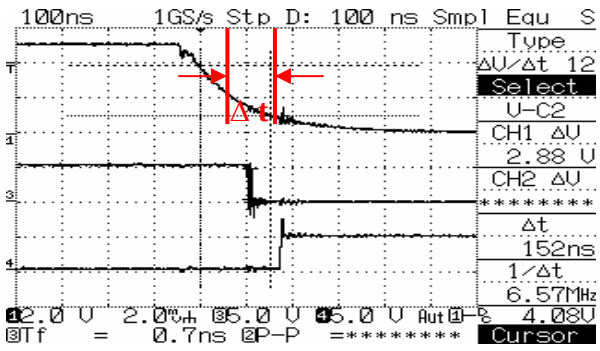


Fig.6 CH1 : SYNC ; CH3 : MOSG-F ; CH4: MOSG-C

Freq. =100KHz

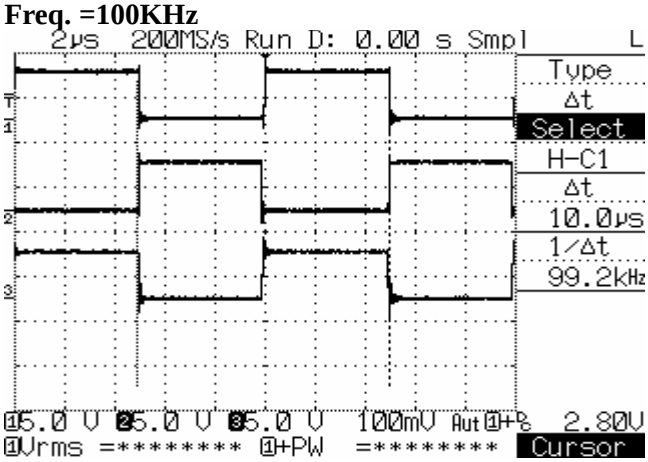


Fig.7 CH1:SYNC INPUT; CH2:MOSG-C; CH3:MOSG-F

Freq. =100KHz

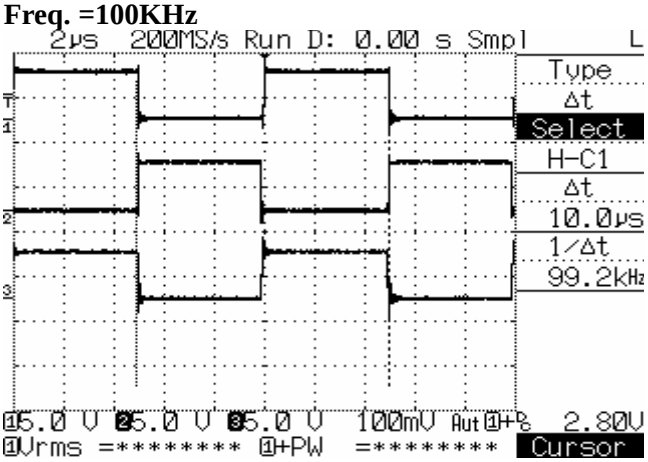


Fig.8 CH1:SYNC INPUT; CH2:MOSG-C; CH3:MOSG-F

SYNC

This pin is sync threshold voltage for SP6002. The Sync input voltage stands between V_{DD} and V_{DD} + 0.5 volts. It is necessary to use a resistor divider if the Sync voltage is much higher than 5 volts. R4 and R5 function as a voltage divider, in which the voltage from the secondary side of the transformer might reach as high as 40V-60V. The maximum allowable voltage for this pin is 7.5 volts. When the voltage is reached above this limit, the IC may suffer permanent damage. The transformer secondary voltage over 7.5V that needs to add the resister divider on this pin. When AC input=90V, adjust the sync high threshold voltage to be larger than 3.9V and sync low threshold voltage to be less than 0.9V. If the input changes to AC input>264V, IC has an internal 7.5V ZENER DIODE that will clamp. It avoids damaging to SP6002.

Note: 1.5Kohm<(R4+R5)<20Kohm

Sync Signal From Function Generator

(1) R4 is removed & function generator is used to force square waveform on pin8. Adjust Sync threshold high voltage>3.9V and sync threshold low voltage<0.9V.
(2) +5V is forced on pin7 (VDD pin).
(3) At the drain of each MOSFET, connect 100ohm to pull up +5V(VDD)
(4) Fig.8 : f = 100Khz ; Fig.9 : f = 200Khz ; Fig.10 : f = 300Khz

Freq. =200KHz

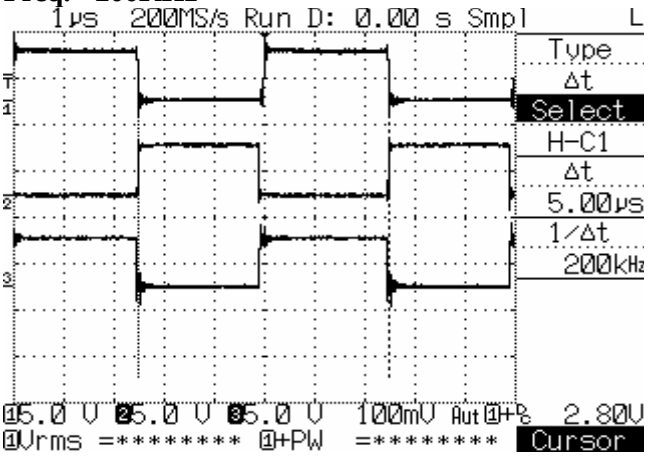


Fig.9 CH1:SYNC INPUT; CH2:MOSG-C; CH3:MOSG-F

Freq. =300KHz

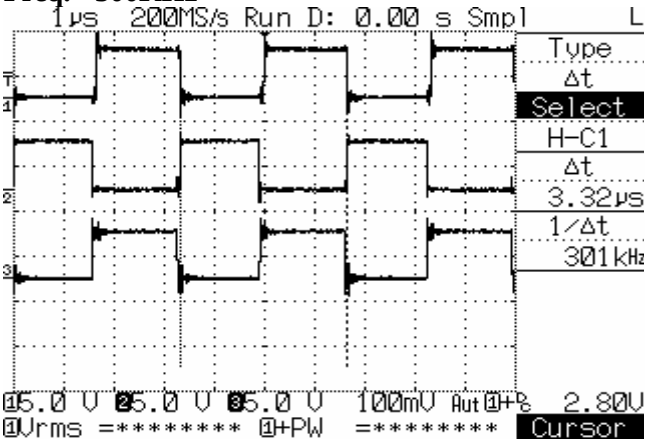


Fig.10 CH1:SYNC INPUT; CH2:MOSG-C; CH3:MOSG-F

Sync Signal From SMPS

(1) At AC input 90V, adjust the resister divider to set sync high threshold>3.9V and sync low threshold<0.9V(pin8).

Note： If the square waveform has been checked already, the probe has to be removed. The probe has nearly 10pf capacitor that will effect “detect slope rate”.

(2) Adjust the R1 resistor value to trigger the gate of MOSFET.

(3) Fine tune the C2 value to get optimum efficiency.

Predictive timing circuit operation (Pred)

The IC operates on the principle of “prediction”. For freewheeling (catch) control applications, the prediction time is defined as time interval from the falling edge of Vgs to the rising edge of the synchronizing signal as shown at Fig.11. The goal is to keep prediction time as short as possible to keep minimum body diode conduction.

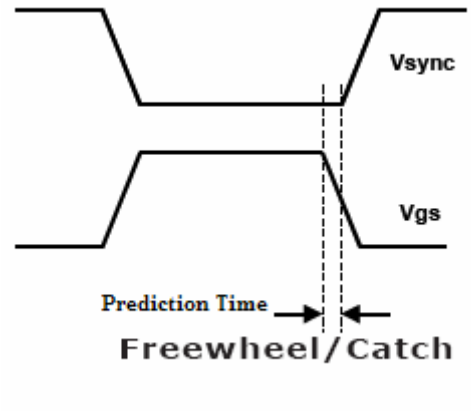


Fig.11 Prediction Time

The Prediction logic uses the previous cycles to control SR operation in the present cycle. The predictive turn OFF time is adjusted by the capacitance on Pred pin. When the actual prediction time is more than that set by the capacitance on Pred pin, the IC reduces the Prediction time in the next cycle. When the actual prediction time is less than that set by the capacitance on Pred pin, the IC increases the prediction time in the next cycle.

The initial time is 100ns for Prediction Time.

MOSG-C and MOSG-F

These two pins connect to the gate of the catch MOSFET and Forward MOSFET. The internal driver capability of SP6002 has dictated the selection of the MOSFET to have Ciss less than 6000 pF. For some applications, it requires to connect two MOSFETs in parallel. Under this circumstance, the Ciss may be over 6000 pF and it is suggested:

(1) To use the Gate Drivers, like IR(IR4427) or TI(UCC27324), between SP6002 and MOSFETs.

(2) To use two SP6002 in parallel.

Power Source

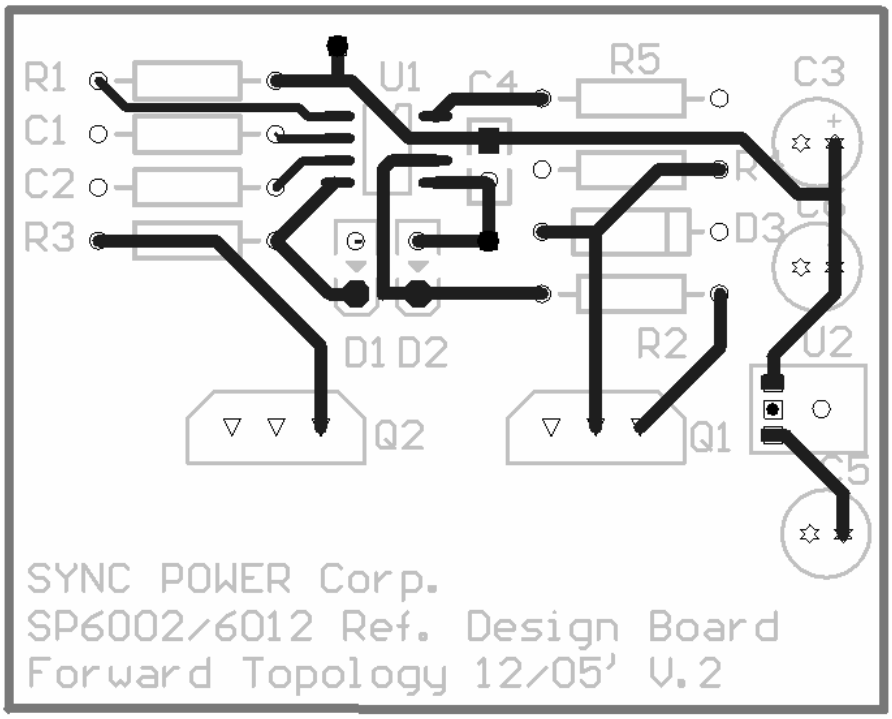
For converters with output voltage higher than 6.5V, the power to SP6002 can be delivered from converter output voltage via a voltage regulator KA7805 or 78L05 as shown in figure 3. An input (0.33uF) and output (0.1uF) capacitor is also required for the voltage regulator. This approach is recommended for voltages from 6.5 volts minimum ripple valley voltage to 35 volts maximum peak voltage.

Some converters have output rated at 5V, the power source for SP6002 could be delievered directly from that source.

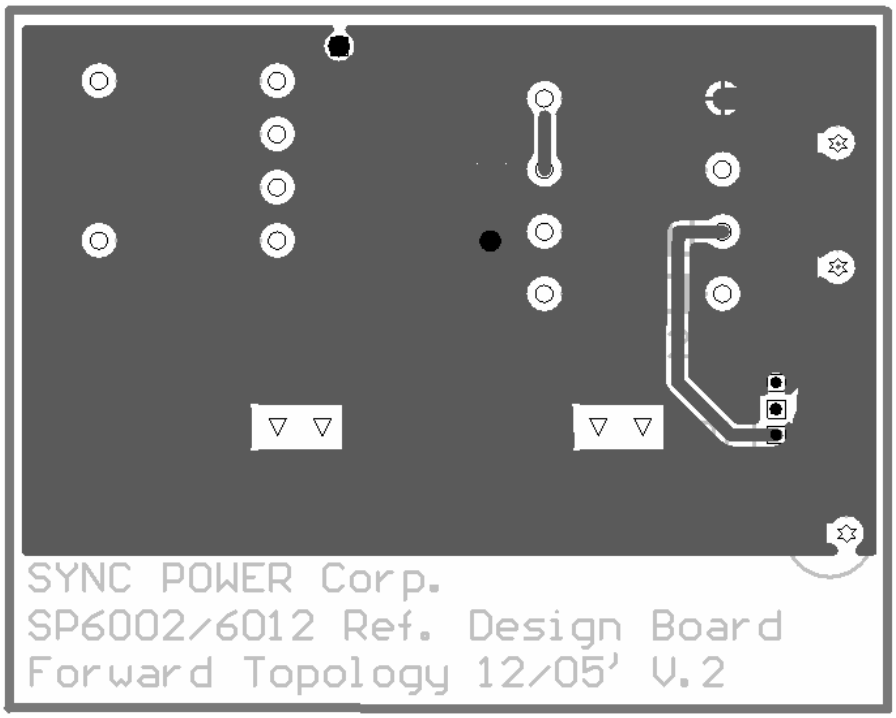
An alternate method is to have a 5.0V secondery wind coil from the transformer.

PCB View

TOP-layer View



Bottom-layer View



Layout notice:

1. A 0.1uf capacitor should be placed as closed as possible to Vdd Pin.
2. The D1 & D2 should be placed next to SP6002.