SYNC POWER CORP.

APPLICATION NOTE AN007

SP6018 SIMPLIFIES IMPLEMENTATION OF SYNCHRONOUS RECTIFIER IN RESONANT CONVERTER

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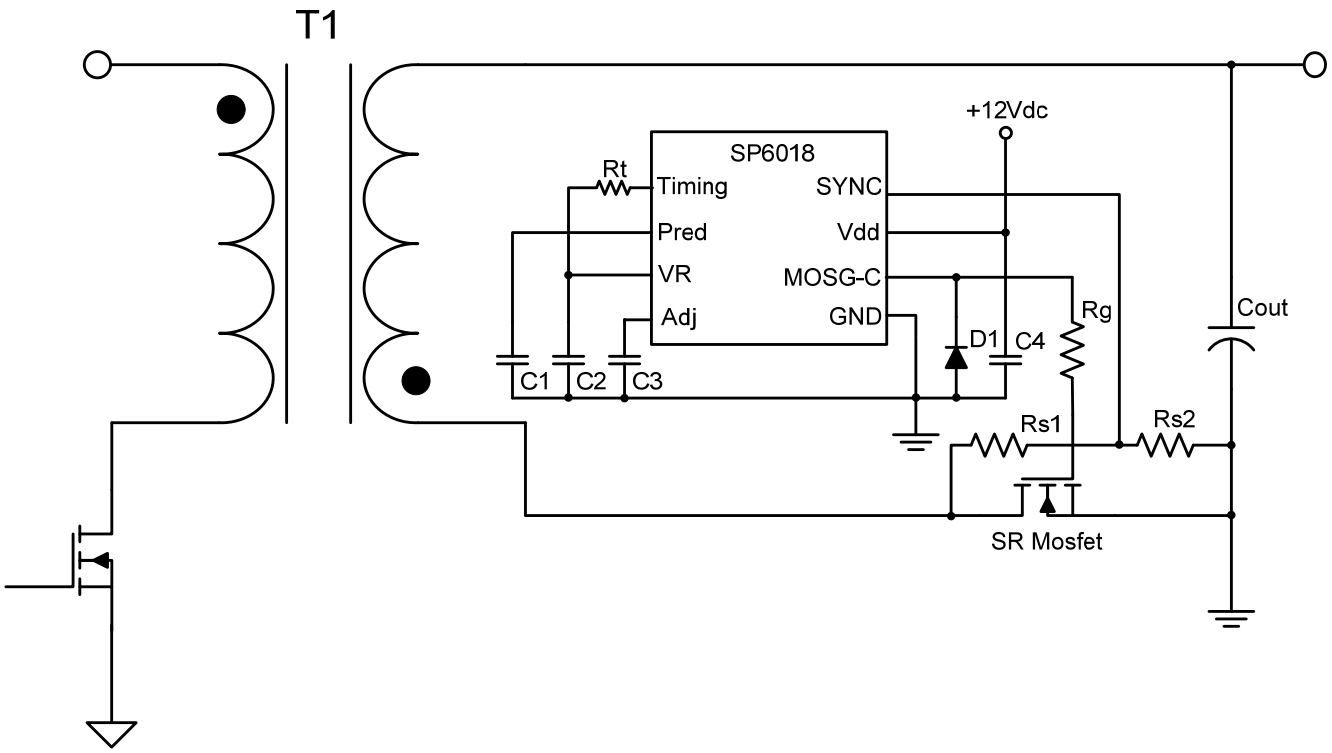
1. Abstract：

The application details of SP6018 for controlling SR MOSFET to operate like a Rectifier as shown in Figure 1 is demonstrated in this application note.

Figure 1. Application Circuit



2. Operation Principles：

SP6018 is an intelligent Synchronous Rectifier Control IC, it controls the ON and OFF sequence of a SR MOSFET (Low Ron) to make the active switch act diode like, to achieve high rectification efficiency.

The SP6018 takes the SR MOSFET drain voltage (Vds) as the synchronize signal to control SP6018 output, which drives the SR Mosfet gate (Vgs). When the Vds of SR MOSFET is high, its Vgs is kept low, and when the Vds is low, SR MOSFET Vgs is kept high. To avoid cross conduction, a predictive dead time is built in between Vgs and Vds to ensure that Vgs is turn OFF prior Vds going high.

SP6018 also has a built-in circuit that senses the dV/dT of the SR MOSFET Vds, which allows it to operate in the Discontinuous Mode (DCM).

3. Pin Configuration:

Figure 2. IC Configuration

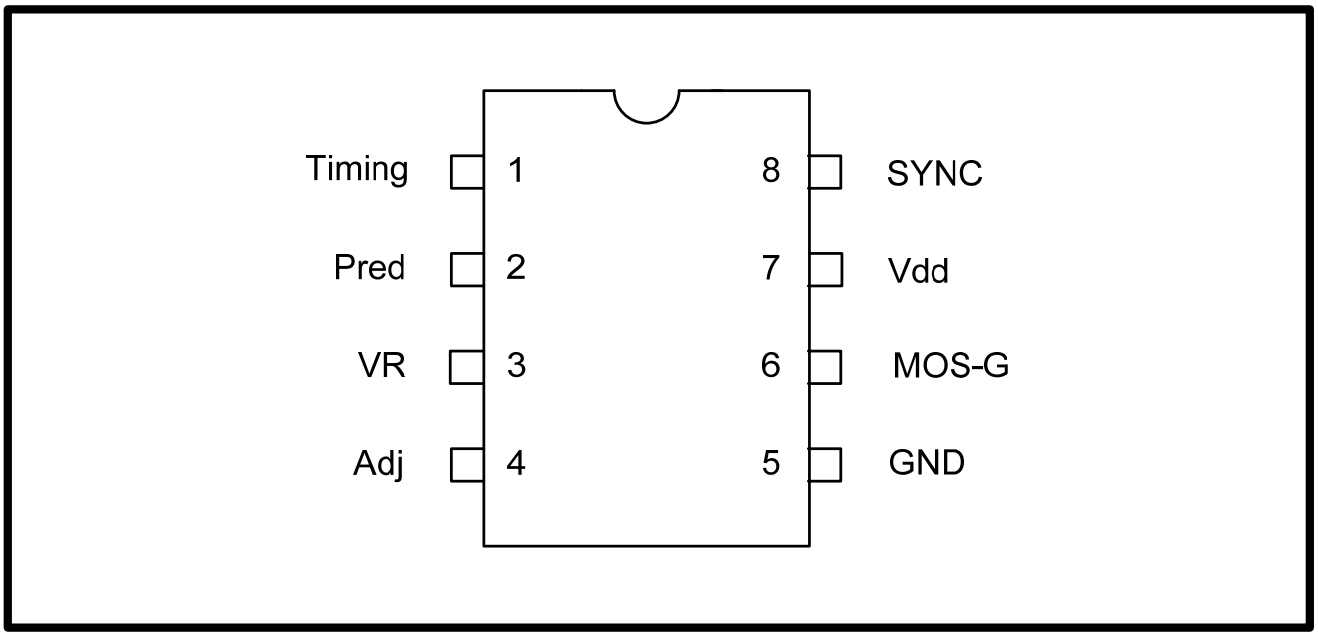
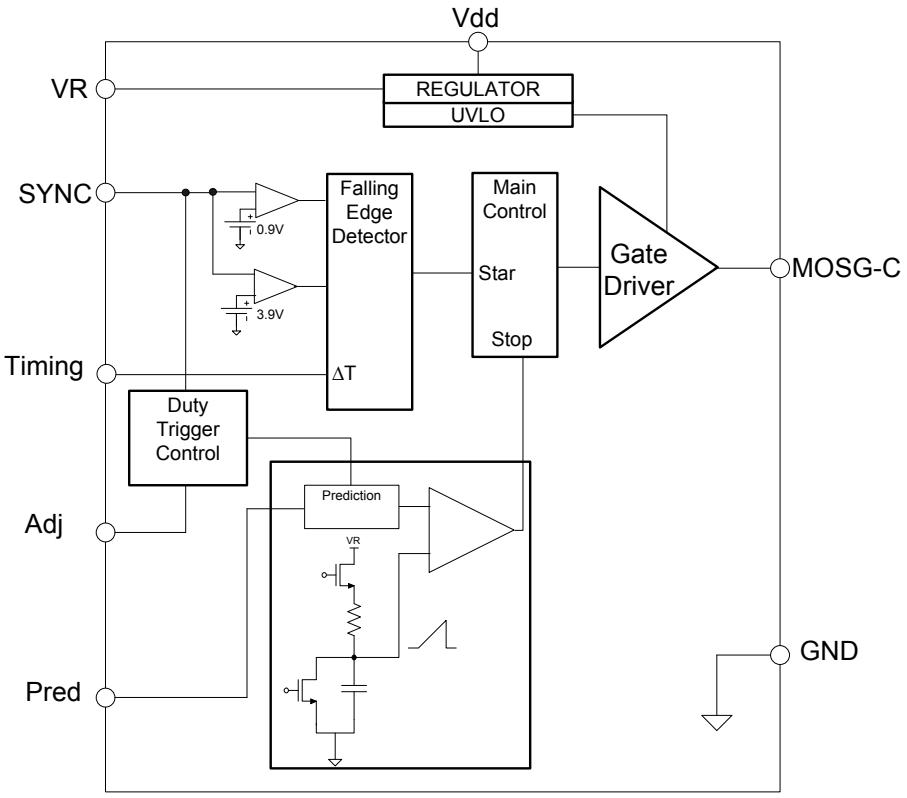


Table 1. Pin Configuration

Pin	Symbol	Description
1	**Timing**	Output (Vgs) Enable Adjustment (for SR MOSFET Activation Based on Load Current)
2	**Pred**	SR MOSFET Vgs and Vds Dead Time Adjustment.
3	**VR**	Internal Reference Voltage.
4	**Adj**	Dynamic Response Sensitivity Adjustment.
5	**GND**	Ground
6	**MOSG-C**	Output for Driving SR Mosfet Gate。
7	**Vdd**	IC Supply Voltage
8	**SYNC**	Synchronous Signal for Connecting to SR MOSFET Vds。

4. Internal Block Diagram：

Figure 3. Internal Diagram



5. Operational Details：

5.1 Supply Voltage and Under Voltage Lock Out (UVLO)：

The suggested supply voltage for SP6018 is between 10.5 and 16 volts; Maximum DC voltage is 17V；Decoupling Capacitor is required and should be proportional to the Ciss of the SR MOSFET.

Under Voltage Lock Out (UVLO) for the supply voltage is 10.8V (UVLO_on=10.5V)

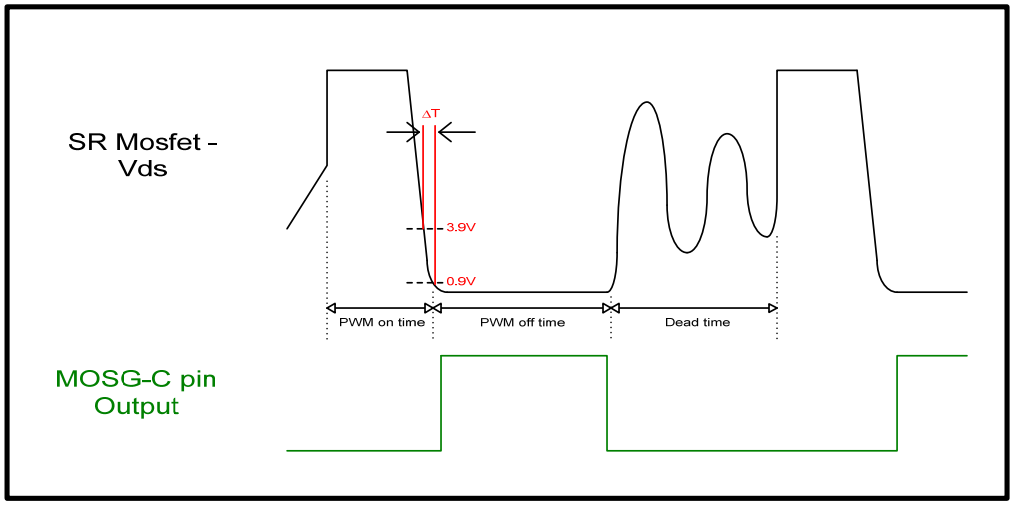
5.2 Obtaining the Synchronous Signal：

SP6018 takes SR MOSFET Drain voltage (Vds) as its synchronous signal via Pin 8, the Sync pin. The Sypc Pin (Pin 8) is clamped at 5V internally, so a resistor divider from Vds is used to obtain the synchronous signal.

5.3 Explanation of Load Current Based SR MOSFET Activation：

There are 2 comparators inside the SP6018 each with a triger voltage of 3.9V and 0.9V respectivly. When SR MOSFET Vds falls through these two trigger voltages at a predetermined time (adjustable at the Timing Pin), the SR MOSFET Vgs is enabled. Otherwise, the SR MOSFET gate is not enabled. This is to avoid false turn ON of the SR MOSFET during DCM mode as shown in Figure 4：

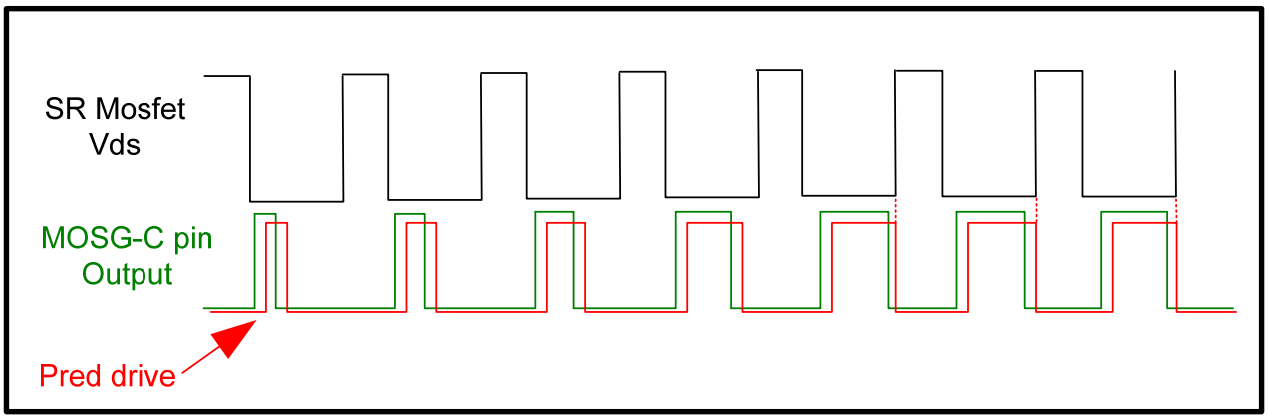
Figure 4. SR MOSFET Activation



5.4 Prediction Control：

SP6018 uses prediction technology to control the Dead Time between SR MOSFET Vgs and Vds. The prediction circuit uses previous cycle‘s timing information for the predictive turn OFF of the Vgs in the current cycle, thus creating a Dead Time for the SR MOSFET as shown in Figure 5.

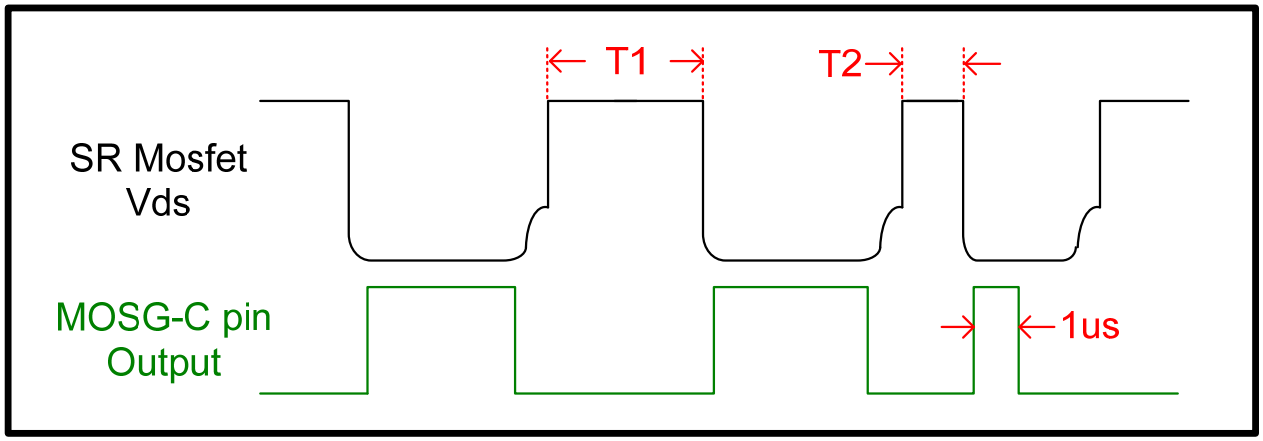
Figure 5. Predication Sequence Waveforms



5.5 Dynamic Response Circuit：

When SP6018 detects a change in PWM ON Time between 2 cycles that is greater than 600ns, (PWM on_time；T1-T2 >600ns), SP6018 would reduce the output (Pin 6) to 1us minimum ON time for the protection of SR MOSFET as shown in Figure 6：

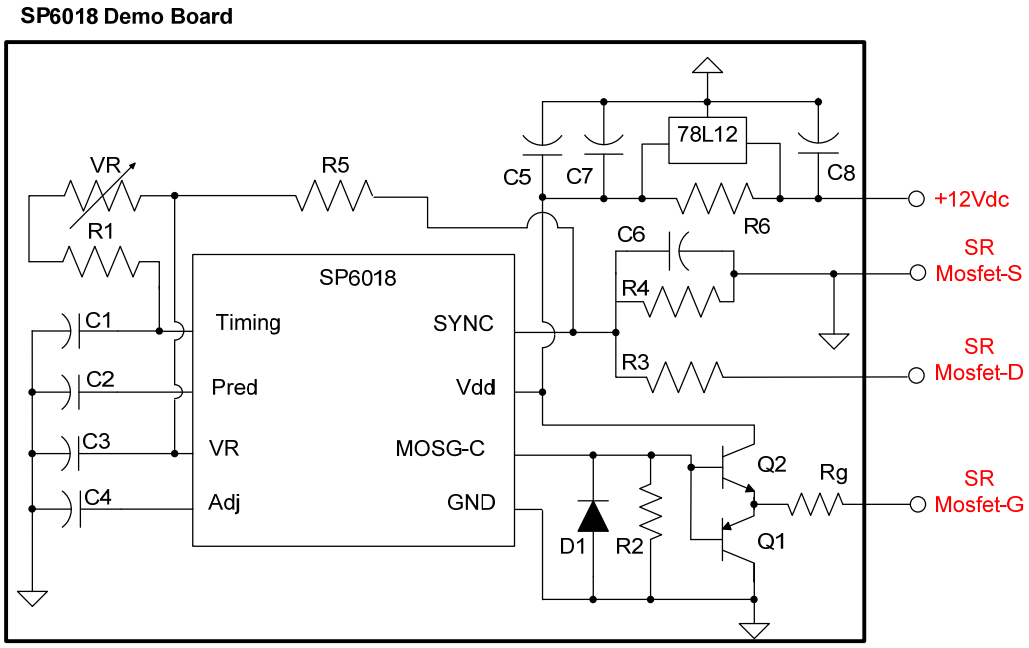
Figure 6. Dynamic Response Adjustment



6.Demo Board Schematic：

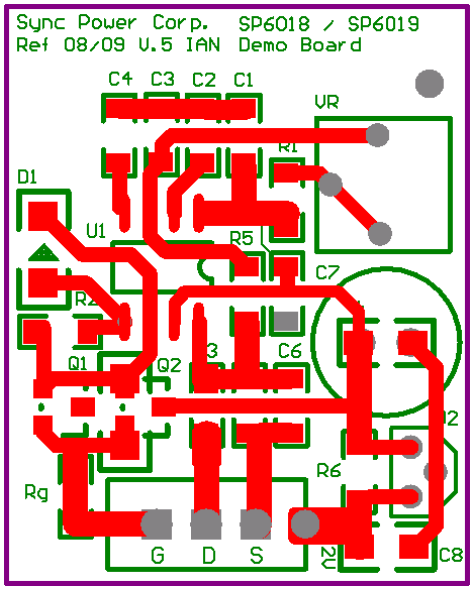
6.1 Demo Board：

Figure 7.

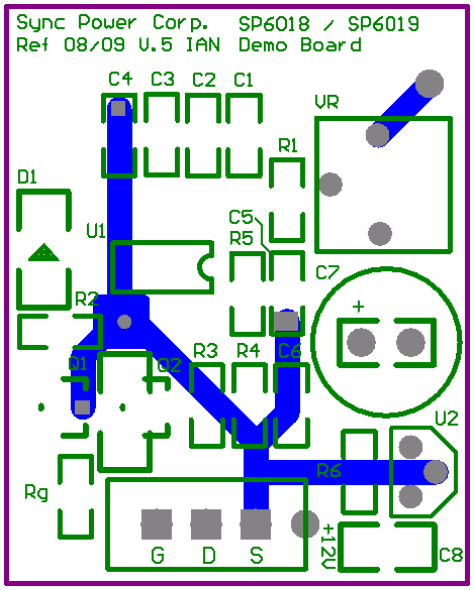


6.2 Demo Board Layout (top、bottom side)

Figure 8. Top side layout



Bottom side layout



6.3 Demo Board Part list：

Table 2. Part list.

P/N	TYPE	FUNCTION
VR、R1	50K、10K	Potentiometer, exchange for fixed resistor after design is completed.
R2	5.1K	Provide Q1 Base Bias
R3、R4	TBD	Resistor divider providing signal for the SYNC pin from SR MOSFET Vds, values To Be Determined, Initial values R3=10K、R4=5.1K。
R5	10K	Pull hi resister for sync signal
R6	5.1	Clamping current resister。
Rg		SR Mosfet Gate protective resistor
C1	104pF	Noise Filter
C2	68pF	for dead time adjustment。C2=68p → dead time set =600~700ns
C3	0.22uF	Capacitor for Internal Reference Voltage (Typ.= +5Vdc)
C4	5~100pF	Dynamic Response Adjustment
C5	0.1uf	Decoupling Capacitor。
C6	5pF~33pF	Noise Filter。
C7、C8	10uF、10uF	Decoupling Capacitor for 78L12
D1	1N4148	MOSFET Gate Protection Diode
Q1、Q2	2907/2222A	External Driver Enhancer
DZ	5.1V	Zener Diode for initial start up supply voltage

6.4 Key Layout Issue：

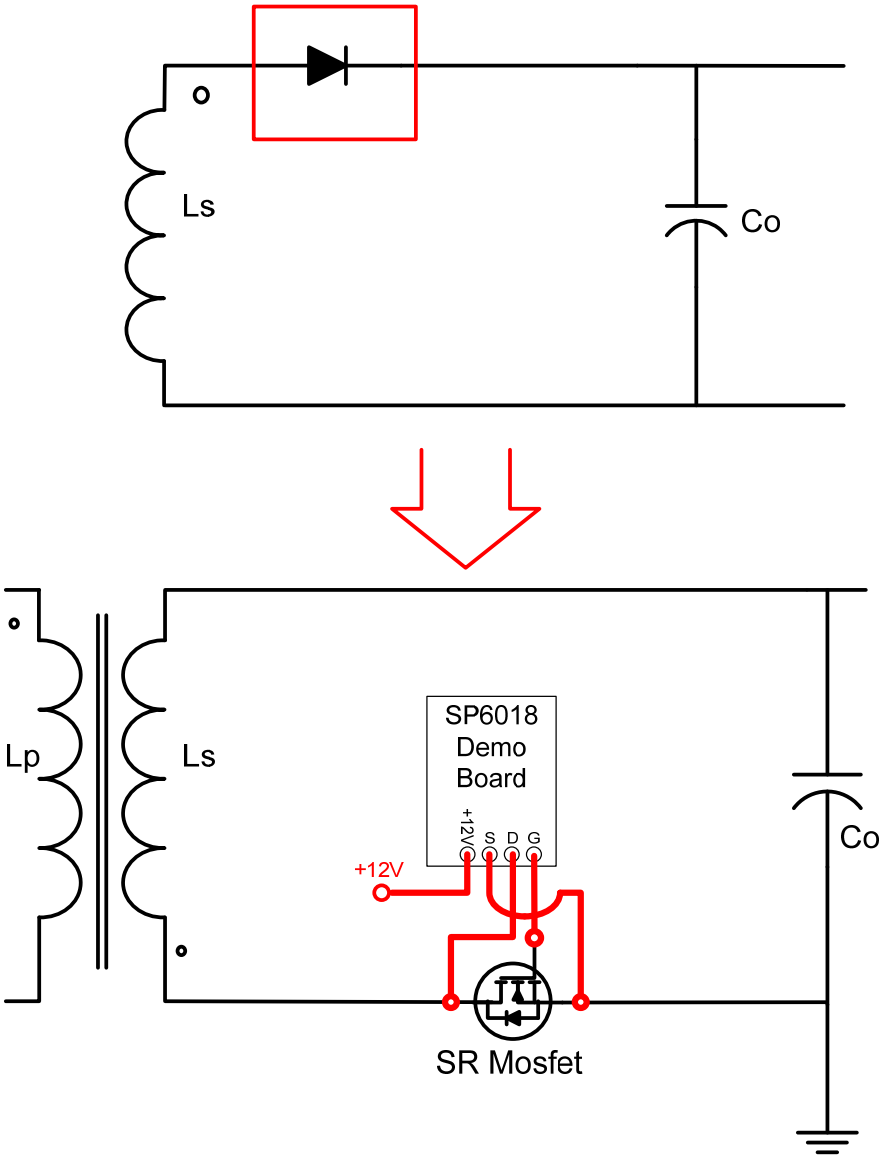
- All ground lines from SP6018 and its auxiliary components should be connected together to Pin 5 before connected to SR MOSFET source.
- PIN 8 SYNC synchronous signal is from SR MOSFET DRAIN through a resistor divider R3、R4。
- SR MOSFET and SP6018 should be as close as possible in layout.
- SP6018 should be far from the transformer in PCB Layout to avoid possible interferences.

7.Application and Adjustments：

7.1 Connection the Demo Board with Your Converter:

First, replace the free-wheel diode with SR MOSFET, then connect the SP6018 Demo Board as shown in Figure 9：

Figure 9. SP6018 Demo Board connections



7.2 Adjusting Demo Board：

- Determine R3(to limit current)、R4(divide voltage) as follows：

  Ex：if secondary side voltage is 30~60V、On Duty(max)=40%、VR pin=5V SYNC pin input max current 3mA。

$$R3_{(min)} = \frac{Vds_{(max)} \text{ X } On\_time_{(max)} - Set\ voltage_{SYNC\ pin}}{Limit\ Current_{SYNC\ pin}}$$

$$R3_{(min)} = \frac{60V \text{ X } 40\% - 5V}{3mA} = 6.33K$$

$$R4_{(min)} = \frac{Set\ voltage_{SYNC\ pin} \text{ X } R3}{Vds_{(min)} - Set\ voltage_{SYNC\ pin}}$$

$$R4_{(min)} = \frac{5V \text{ X } R3}{30V - 5V} = 1.267k$$

※ Initial values can be set at R3=10K、R4=5.1K。

- The RT on Demo Board is a potentiometer. The smaller the RT, the easier to activate SR MOSFET as shown in Figure 10.

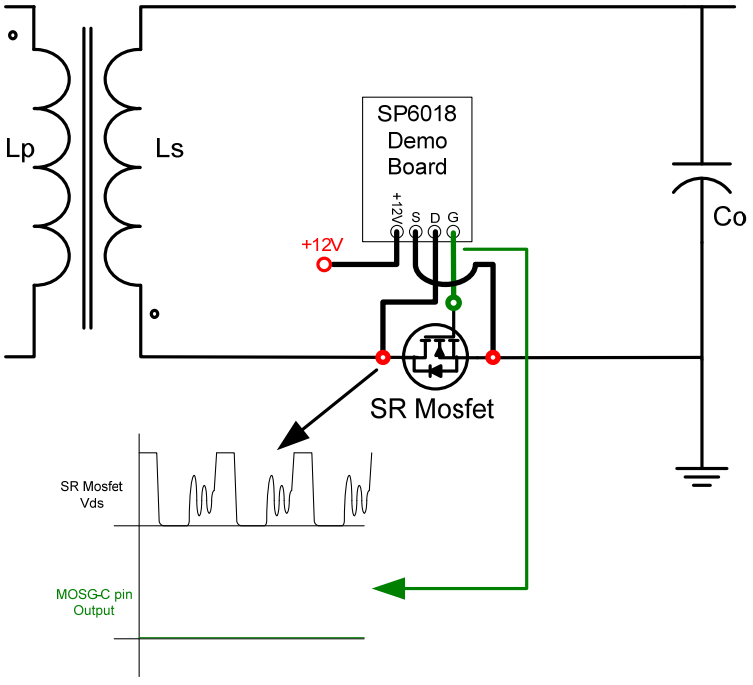


Figure 10.

- Put the converter in light load, and adjust RT on the Demo Board to the max. SP6018 PIN 6 should have no output and the SR MOSFET is not activated, as shown in Figure 10.

- Increase the converter load to about 1A, then adjust RT until SP6018 PIN 6 has output as shown in Figure 11.

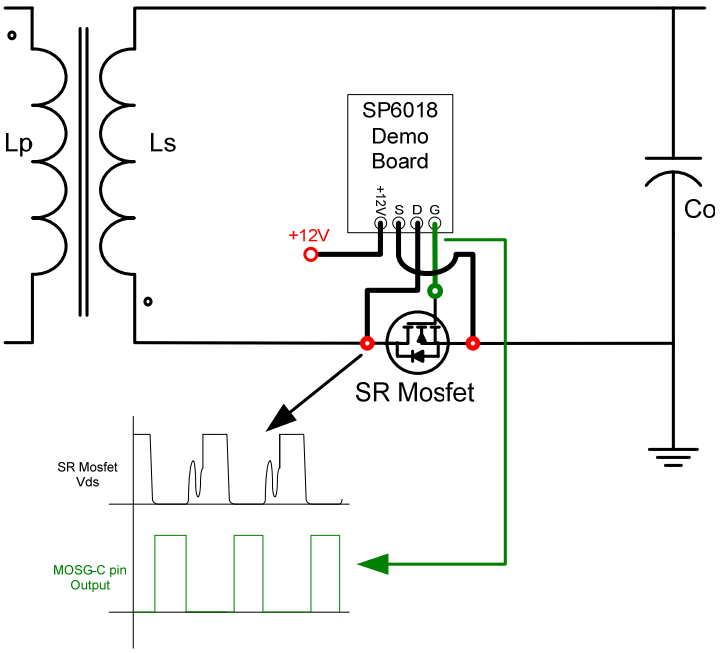
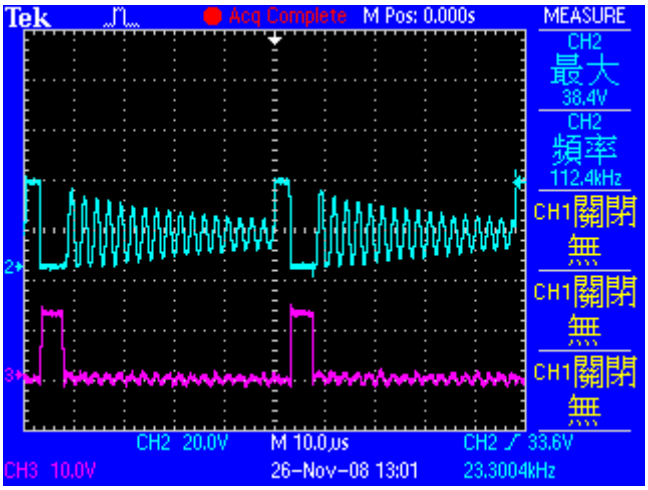


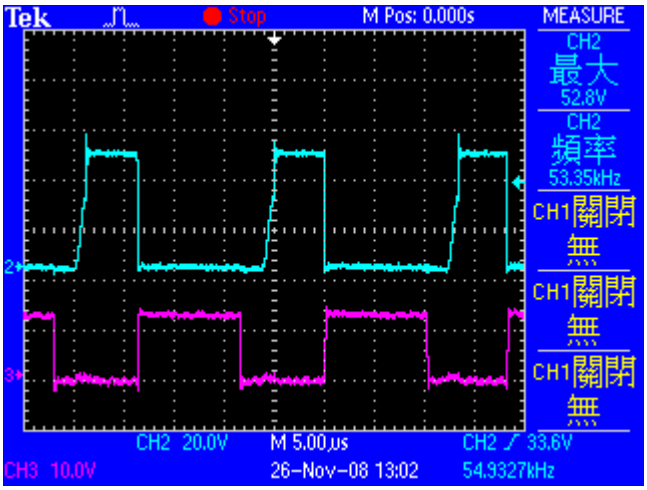
Figure 11

- Note the resistance of the Potentiometer, and replace the Potentiometer with a fix resistor. Thus, complete the SR adjustment.

- Scope waveforms for a 12V/6.6A converter is shown below：



Io=0.3A

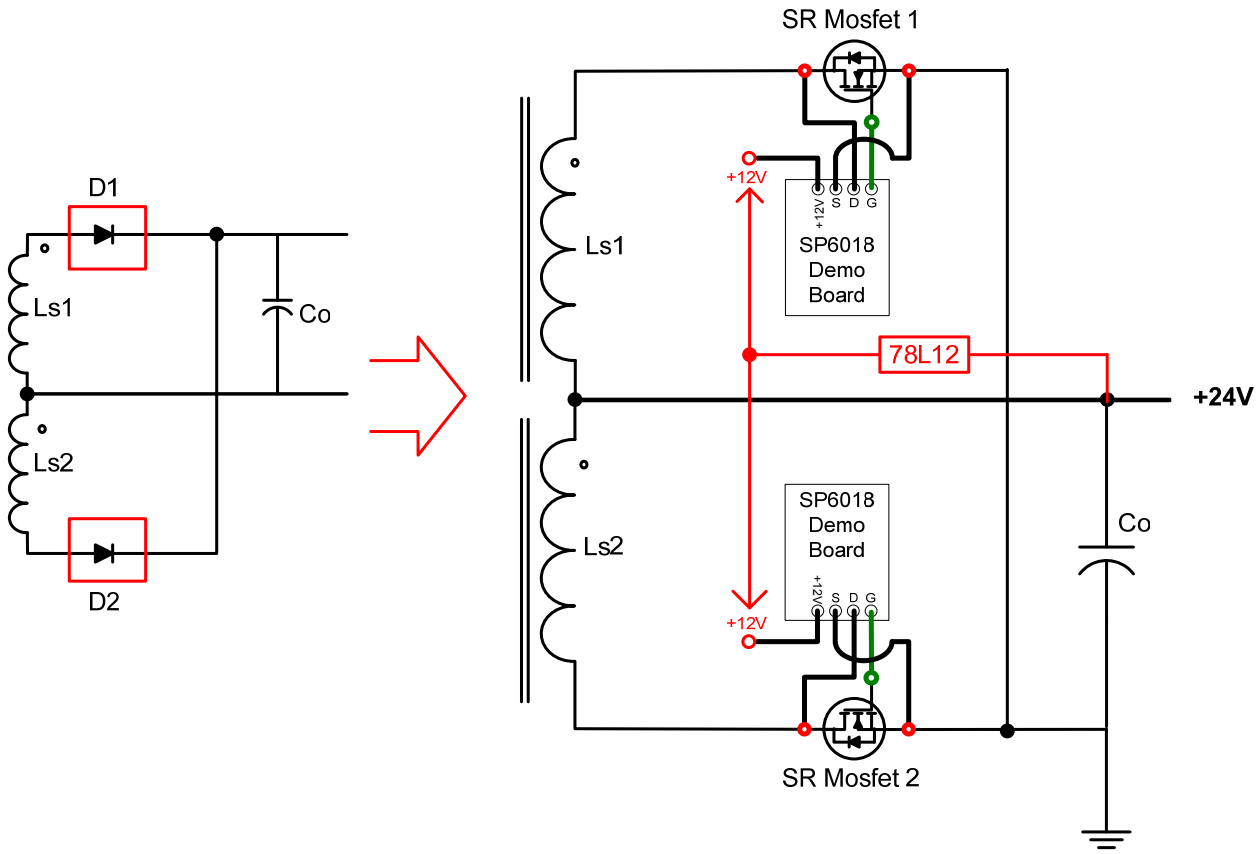


Io=7A

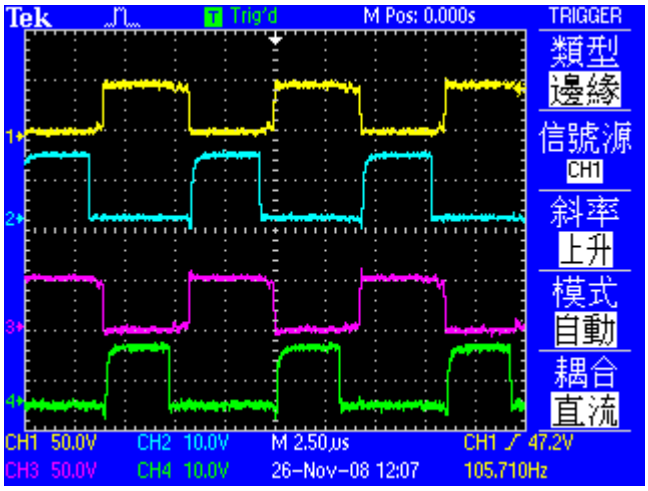
CH2-SR Mosfet Vds、CH3-SR Mosfet Vgs

7.3 LLC application schematic

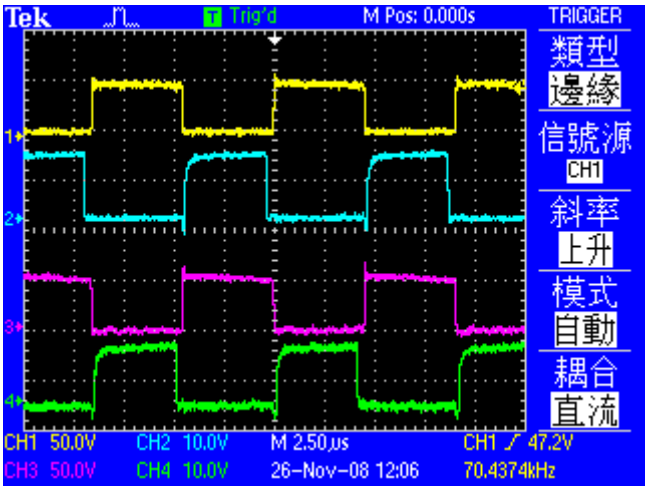
Figure 12.



- Scope waveforms of 24V/7A LLC converter.



Io=0.3A



Io=7A

CH1-SR Mosfet1 Vds、CH2-SR Mosfet1 Vgs、CH3-SR Mosfet2 Vds、CH4-SR Mosfet2 Vgs

SYNC Power Corporation
9F-5, No.3-2, Park Street
NanKang District (NKSP), Taipei, Taiwan, 115, R.O.C
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
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