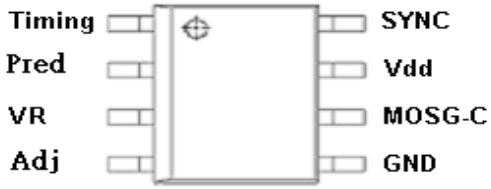
SP6019D
Synchronous Rectifier Driver

DESCRIPTION
The fundamental of SP6019D synchronous rectifier (SR) driver IC is based on our U.S. patented methods that utilize the principle of "prediction" logic circuit. The IC deliberates previous cycle timing to control the SR in present cycle by "predictive" algorithm that makes adjustments to the turn-off time, in order to achieve maximum efficiency and avoid cross-conduction at the same time. SP6019D is specially suitable for Forward and DC/DC Module.

APPLICATION
- Servers & workstations
- Storage area network power supplies
- Telecommunication converters
- Embedded systems
- Industrial & commercial systems using high current processors
- DC/DC Power Module

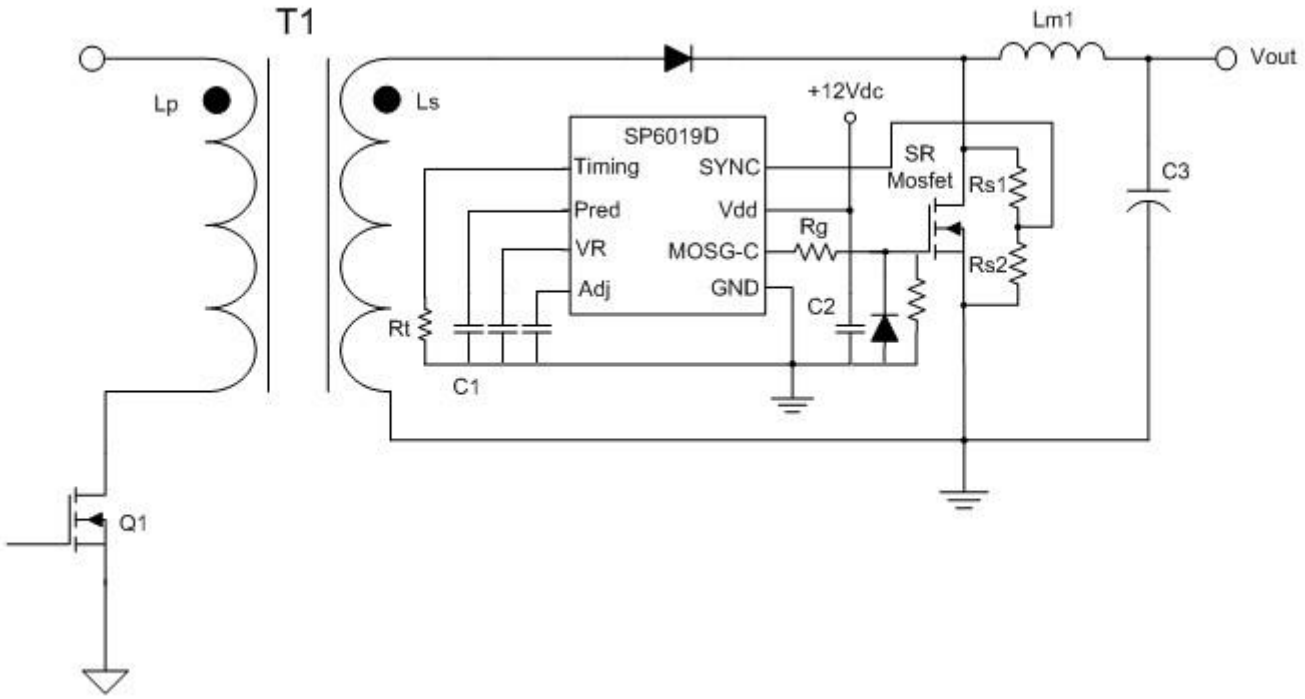
FEATURES
- Offers efficiency improvement over Schottky Diode (depends on drive configuration of the SR).
- Drives all Power MOSFET.
- Prediction gate timing control.
- Minimum MOSFET body diode conduction.
- Operating at high switching frequency.
- Synchronize to transformer secondary voltage waveform.
- Linear setting of timing function.
- SOP-8 Package

PIN CONFIGURATION (SOP-8)


PART MARKING


A : Lot Code
B : Date Code

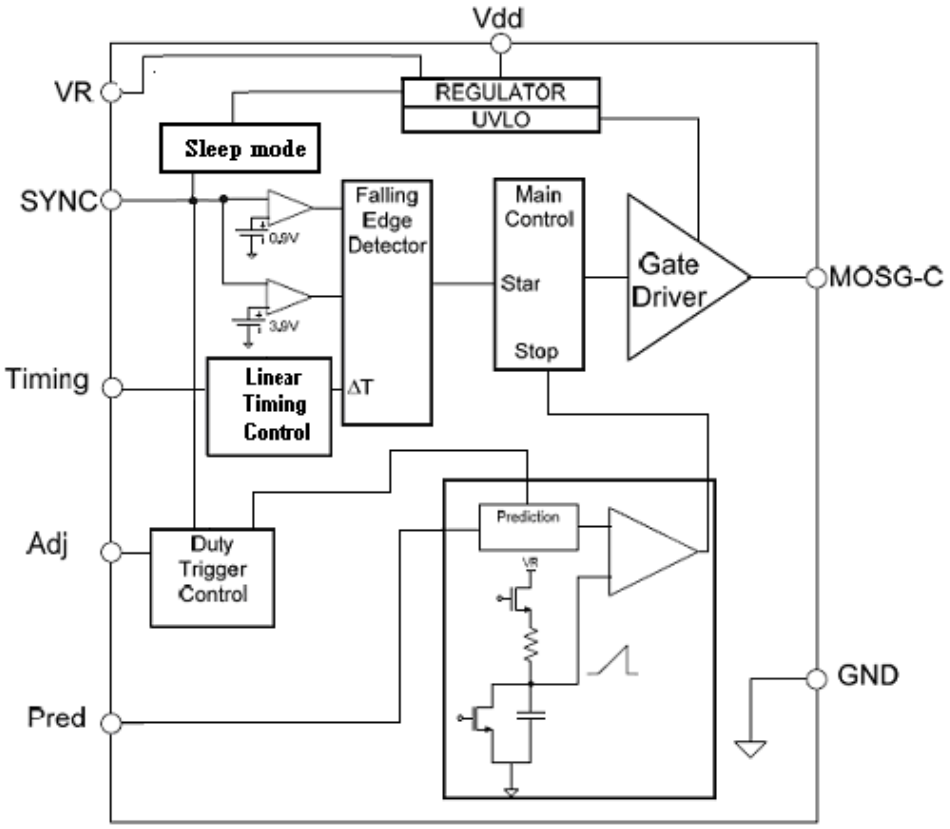
TYPICAL APPLCATION CIRCUIT



PIN DESCRIPTION

Pin	Symbol	Description
1	Timing	Discontinuous current filter timing adjustment resistor connection.
2	Pred	Capacitor to store previous cycle timing for SR MOSFET.
3	VR	Voltage Regulator.
4	Adj	Trigger point adjustment for Dynamic state.
5	GND	Ground connection.
6	MOSG-C	Catch MOSFET gate drive.
7	Vdd	DC supply voltage.
8	SYNC	Synchronized signal from the V_{DS} of SR MOSFET.
9	GND	Ground, Exposed Pad

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Part Marking
SP6019DS8RGB	SOP-8	SP6019D
SP6019DS8TGB	SOP-8	SP6019D

※ SP6019DS8RGB : Tape Reel ; Pb – Free ; Halogen - Free

※ SP6019DS8TGB : Tube ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS (TA=25℃, unless otherwise specified.)

The following ratings designate persistent limits beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{dd}	DC Supply Voltage	16	V
I_{OUT}	Peak Source Current (Pulsed)	2.0	A
	Peak Sink Current (Pulsed)	2.0	A
P_D	Power Dissipation @ T_A=85℃ SOP-8 (*)	0.25	W
P_D	Power Dissipation @ TA=85℃ TDN8 (*)	1.8	W
T_J	Operating Junction Temperature Range	-40 to125	℃
T_{STG}	Storage Temperature Range	-40 to 150	℃
T_{LEAD}	Lead Soldering Temperature for 5 sec.	260	℃

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
RθJC	Thermal Resistance Junction – Case SOP-8 (*)	45	℃/W
RθJC	Thermal Resistance Junction - Case TDN8 (*)	8	℃/W

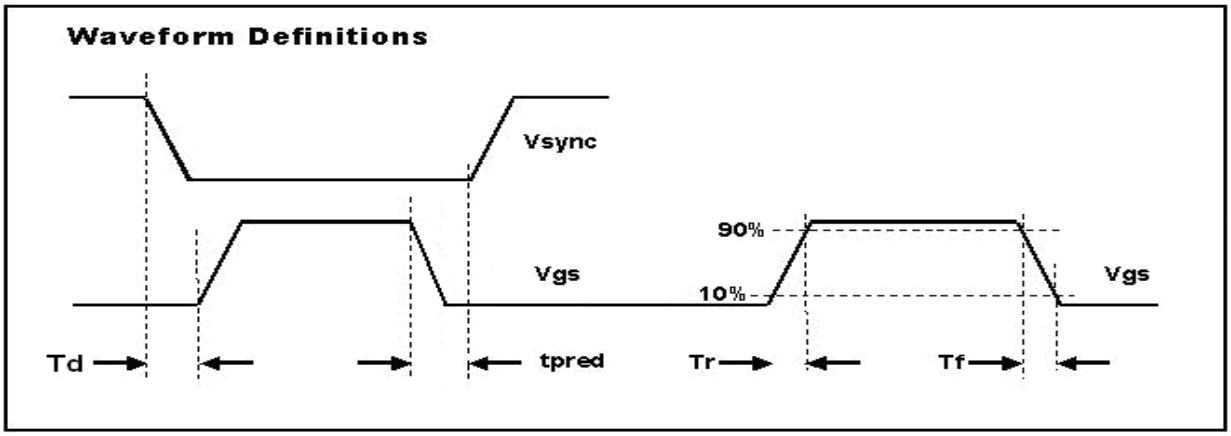
(*) The power dissipation and thermal resistance are evaluated under copper board mounted with free air conditions.

ELECTRICAL CHARACTERISTICS

(T_A=25℃, V_{dd}=12V, Freq. =50 KHz, Duty Cycle=50%, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY INPUT						
IDD	Supply current	No load		0.15		mA
		V_{SYNC}=0V, Vdd on		3	4	mA
Vdd	Supply voltage	Idd peak < 2A			16	V
Vdd on	Enable voltage		7.8	8.2	8.6	V
Vdd hysteresis	Enable voltage			0.25	0.5	V
Vovp	Over voltage protection		15.5	16.5	17.5	V
Vovp hystersis				0.3		V
SYNC REFERENCE (SYNC)						
Vshth	SYNC high threshold		3.5	3.9		V
Vslth	SYNC low threshold			0.9	1.2	V
Vsync	SYNC wake-up voltage	Isync=3mA	9		16	V
Isync	SYNC input current				3	mA
Voltage Regulator REFERENCE (VR)						
VR	voltage		5.2		5.4	V
IVR	VR Output Current				50	mA
ON TIME DUTY SETUP (PIN 6)						
Ton-time				26	32	us
MOSFET GATE DRIVER (MOSG-C)						
Voh	Output high voltage	Io = -200mA	10.5	11.0		V
Vol	Output low voltage	Io = 200mA		0.5	0.8	V
Td	Propagation delay	No load	25	50	155	ns
Tpred		No load		120		ns
Tr	Rise time	Load = 1nF (*)		10	25	ns
Tf	Fall time	Load = 1nF (*)		10	25	ns
Dynamic Protect						
Dt	Dynamic variable	Pin 4 open		600		ns
Ton-min	MOSG-C on time	PWM adjusts time > Dt		0.5		us

(*) Tr & Tf are measured among 10% and 90% of starting and final voltage.



PERFORMANCE CHARACTERISTICS (T_A=25℃, unless otherwise specified.)

Figure 1: Supply Current VS Supply Voltage

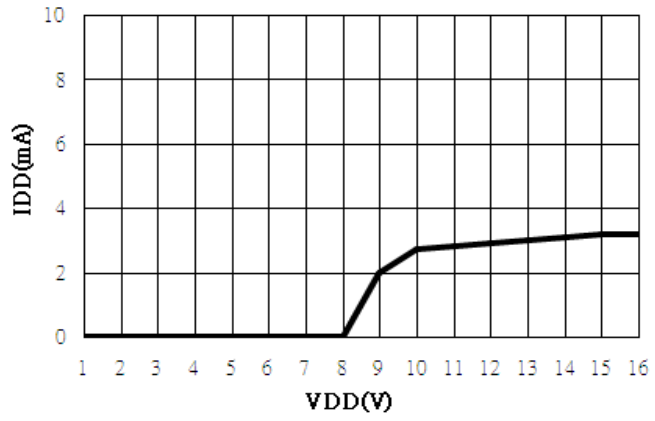


Figure 2: VR Voltage VS Supply Voltage

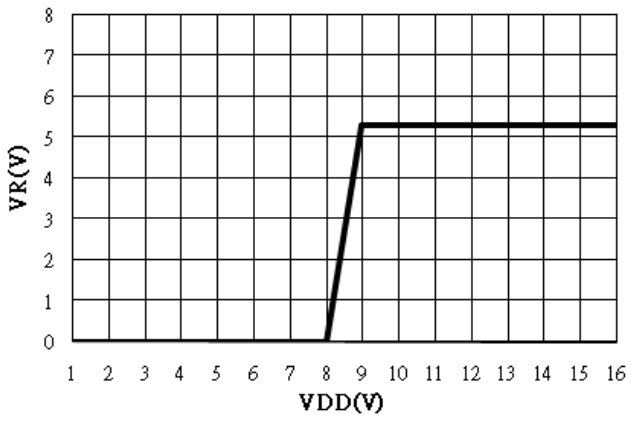


Figure 3: Tpred VS Cpred

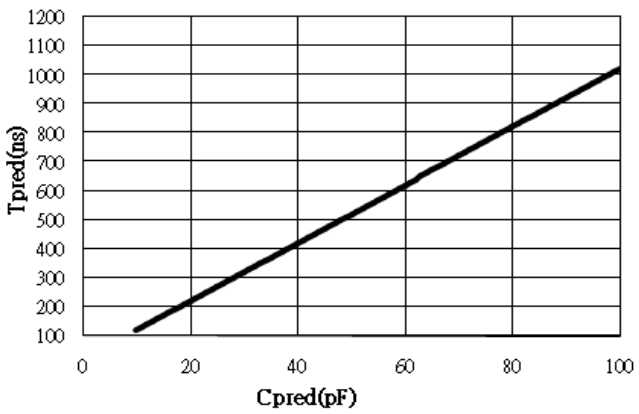


Figure 4: Dynamic time VS C adj (pF)

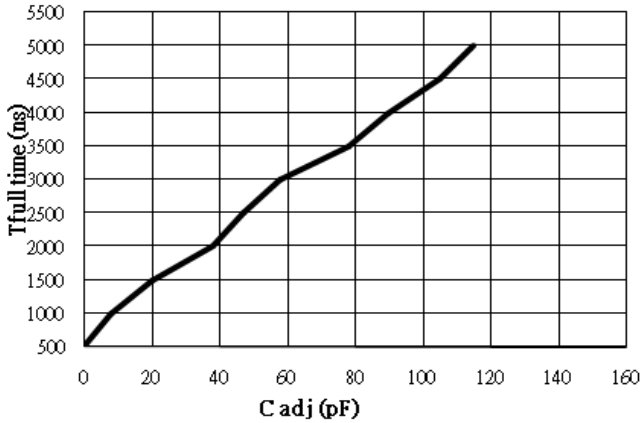


Figure 5: Output Fall Time VS Load Capacitor

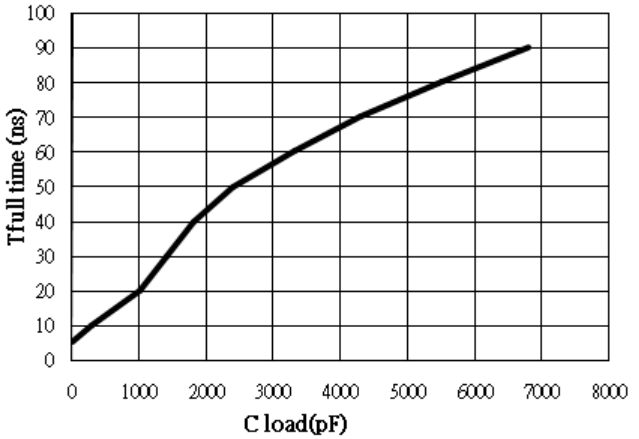


Figure 6: Timing RT VS dt (ns)

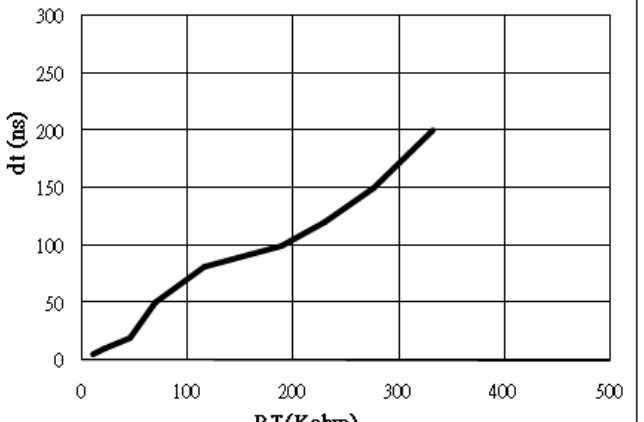
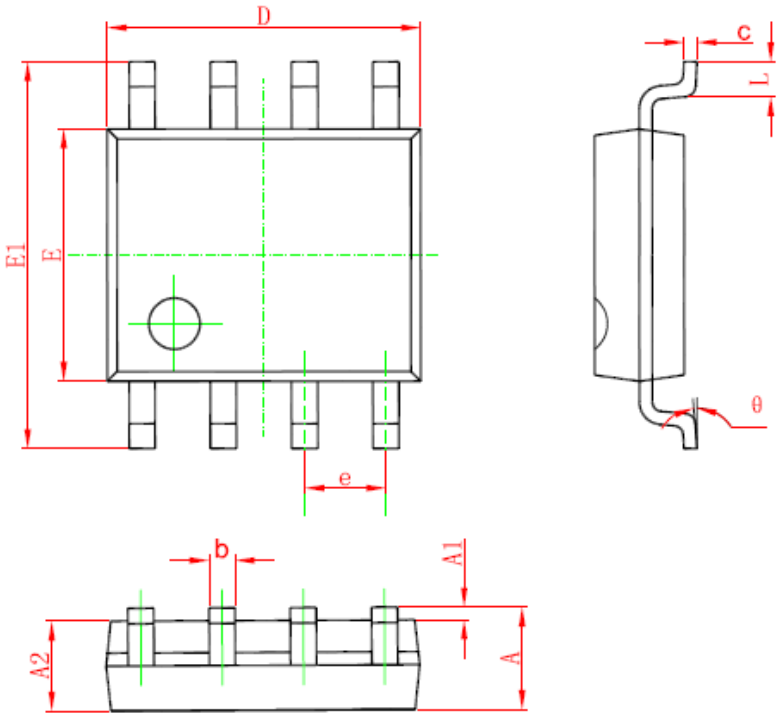


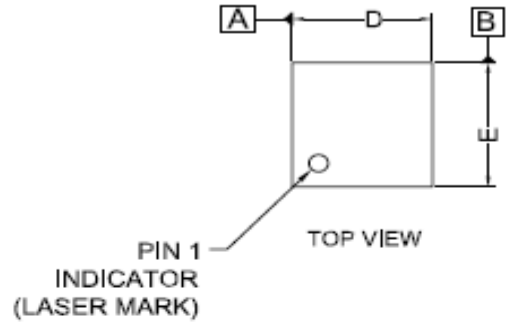
*Fig. 1 : No Load ; No SYNC
*Fig. 3 : Frequency = 100 kHz
*Fig. 4~5 : Frequency = 65 kHz.
*Fig. 6 : The falling time of negative edge from 3.9V to 0.9V

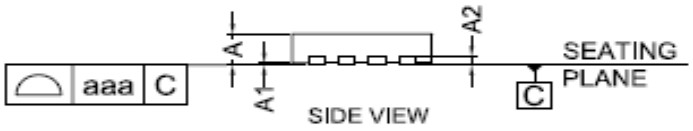
SOP- 8 PACKAGE OUTLINE

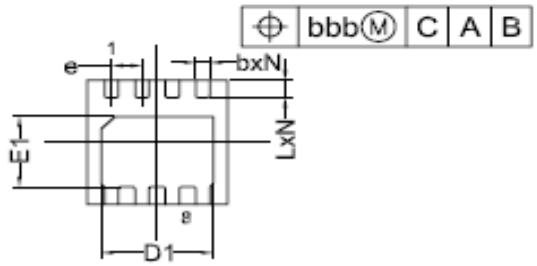


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TDFN3X3- 8LC PACKAGE OUTLINE







BOTTOM VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0,70	0,75	0,80
A1	0,00	0,02	0,05
A2		0,203	
b	0,25	0,30	0,35
D	2,90	3,00	3,10
D1	2,35	2,40	2,45
E	2,90	3,00	3,10
E1	1,65	1,70	1,75
e		0,65BSC	
L	0,37	0,42	0,47
N		8	
aaa		0,08	
bbb		0,10	

NOTES:
1.CONTROLLING DIMENSIONS ARE IN MILLIMETERS(ANGLES IN DEGREES)
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS THE TERMINALS.

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