SPE1211
Single-Line ESD Protection Array

DESCRIPTION

The SPE1211 are designed by TVS device that is to protect sensitive electronics from damage or latch-up due to ESD. They are designed for use in applications where board space is at a premium. SPE1211 will protect single line, and may be used on line where the signal polarities swing above and below ground.

SPE1211 offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

SPE1211 may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SOD-523 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

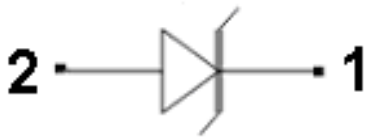
APPLICATIONS

- Cellular Handsets and Accessories
- Cordless Phone
- PDA
- Notebooks and Handhelds
- Portable Instrumentation
- Digital Cameras
- MP3 Player

FEATURES

- Transient protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Protects single I/O lines
- Working voltage: 12V
- Low leakage current
- Low operating and clamping voltages

PIN CONFIGURATION (SOD-523)



PART MARKING

SPE1211
Single-Line ESD Protection Array

ORDERING INFORMATION

Part Number	Package	Part Marking
SPE1211D52RG	SOD-523	A
SPE1211D52RGB	SOD-523	A

※ SPE1211D52RG : Tape Reel ; Pb – Free
※ SPE1211D52RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power (tp = 8/20 μs)	Ppk	300	W
Maximum Peak Pulse Current (tp = 8/20 μs)	Ipp	15	A
ESD per IEC 61000 – 4 – 2 (Air)	Vpp	±15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	Vpp	±8	KV
Operating Junction Temperature	T_J	-55 ~ 125	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃
Lead Soldering Temperature	T_L	260 (10sec)	℃

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	It = 1mA	13.3			V
Reverse Leakage Current	I_R	V_{RWM} = 12V , T=25℃			1	μA
Clamping Voltage	V_C	Ipp = 5A , tp = 8/20 μs			19	V
Clamping Voltage	V_C	Ipp =15A , tp = 8/20 μs			25	V
Junction Capacitance	Cj	Between I/O Pin and GND V_R = 0V , f = 1MHz			100	pF

TYPICAL CHARACTERISTICS

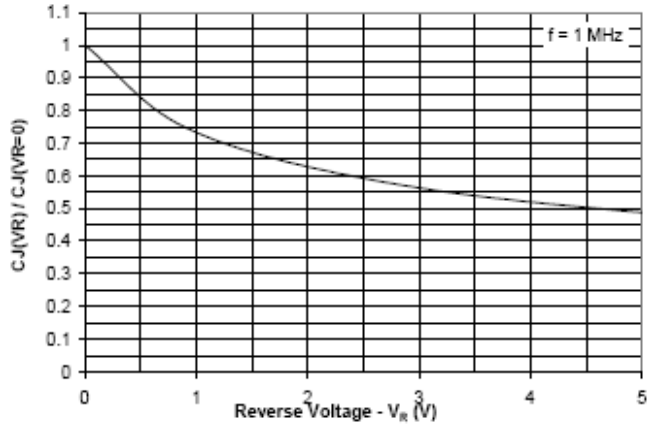


Fig 1 : Junction Capacitance V.S Reverse Voltage Applied

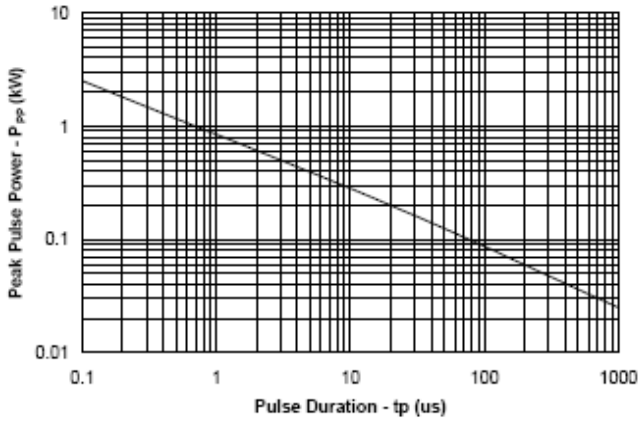


Fig 2 : Peak Plus Power V.S Exponential Plus Duration

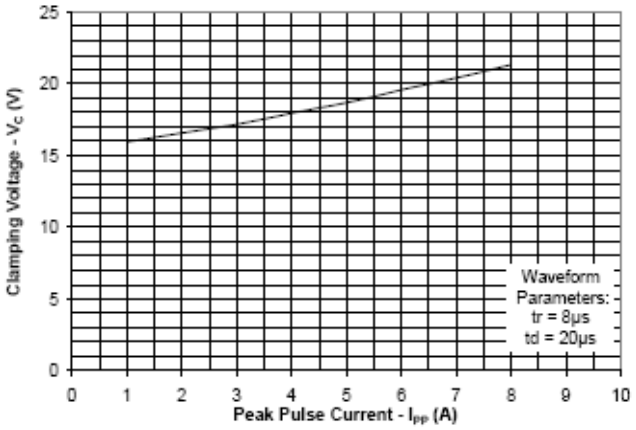


Fig 3 : Clamp Voltage V.S Peak Pulse Current

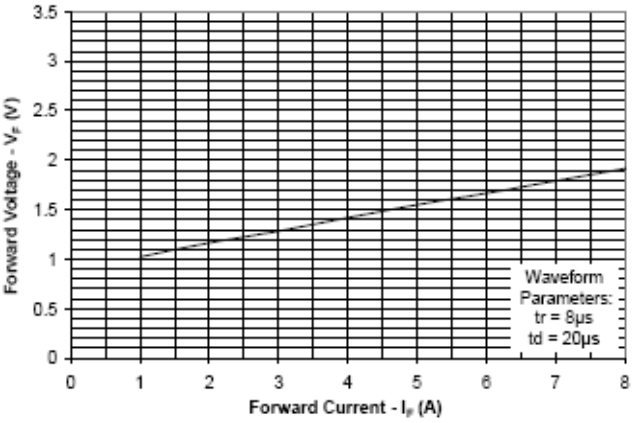


Fig 4 : Forward Voltage Drop V.S Peak Forward

APPLICATION NOTE

Device Connection Options Circuit Diagram

These TVS diodes are designed to protect one data, I/O, or power supply line. The device is unidirectional and may be used on lines where the signal polarity is above ground. The cathode band should be placed towards the line that is to be protected.

Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

★ Place the TVS near the input terminals or connectors to restrict transient coupling.

★ Minimize the path length between the TVS and the protected line.

★ Minimize all conductive loops including power and ground loops.

★ The ESD transient return path to ground should be kept as short as possible.

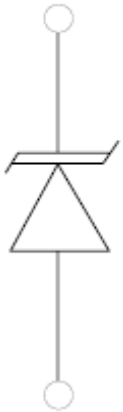
★ Never run critical signals near board edges.

★ Use ground planes whenever possible.

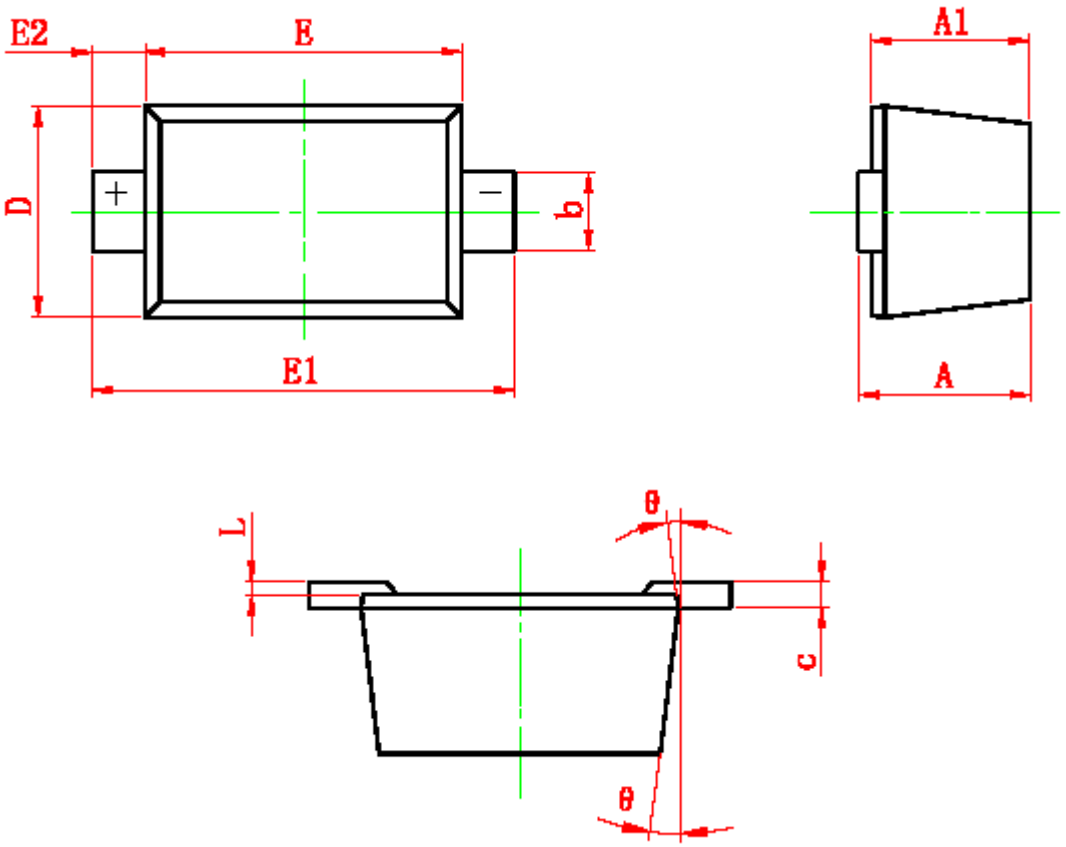
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Circuit Diagram



SOD-523 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.510	0.770	0.020	0.031
A1	0.500	0.700	0.020	0.028
b	0.250	0.350	0.010	0.014
c	0.080	0.150	0.003	0.006
D	0.750	0.850	0.030	0.033
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
E2	0.200 REF		0.008 REF	
L	0.010	0.070	0.001	0.003
θ	7° REF		7° REF	

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