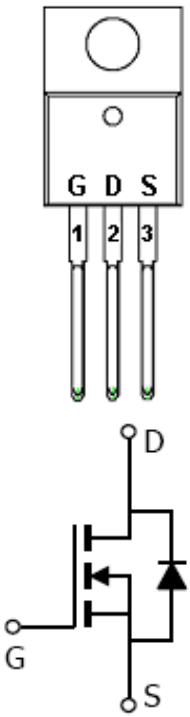
SPN120T15
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN120T15 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

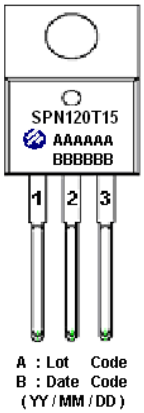
FEATURES
- 150V/120A, $R_{DS(ON)}$=10.5mΩ@V_{GS}=10V
- High density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-220 package design

APPLICATIONS
- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

PIN CONFIGURATION
TO-220



PART MARKING



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N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN120T15T220TGB	TO-220-3L	SPN120T15

※ SPN120T15T220TGB : Tube ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	150	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	120	A
	T_A=100℃		85	
Pulsed Drain Current		I_{DM}	400	A
Avalanche Energy, Single Pulse @ L=0.4mH, T_A=25℃		E_{AS}	845	mJ
Power Dissipation @ T_A=25℃		P_D	333	W
Operating Junction Temperature		T_J	-55/175	℃
Storage Temperature Range		T_{STG}	-55/175	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	60	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V T_J=25℃			1	uA
		V_{DS}=150V,V_{GS}=0V T_J=100℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=20A		8.8	10.5	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		90		S
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=75V, V_{GS}=10V I_D= 20A		66		nC
Gate-Source Charge	Q_{gs}			11		
Gate-Drain Charge	Q_{gd}			24		
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V f=1MHz		4770		pF
Output Capacitance	C_{oss}			340		
Reverse Transfer Capacitance	C_{rss}			92		
Turn-On Time	$t_{d(on)}$	V_{DD}=75V, V_{GS}=10V I_D=20A, R_G=10Ω		17		nS
	t_r			56		
Turn-Off Time	$t_{d(off)}$			30		
	t_f			28		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

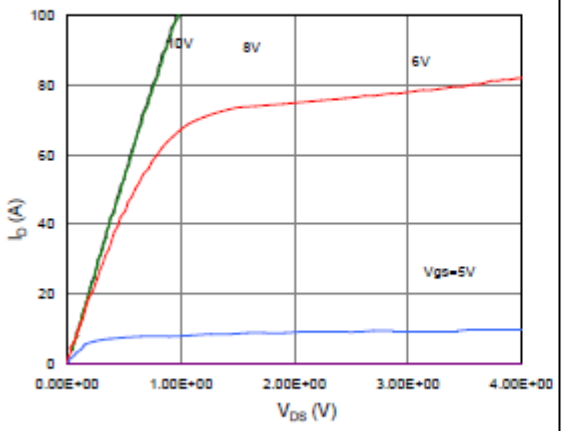


Figure 2. On-Resistance vs. Gate-Source Voltage

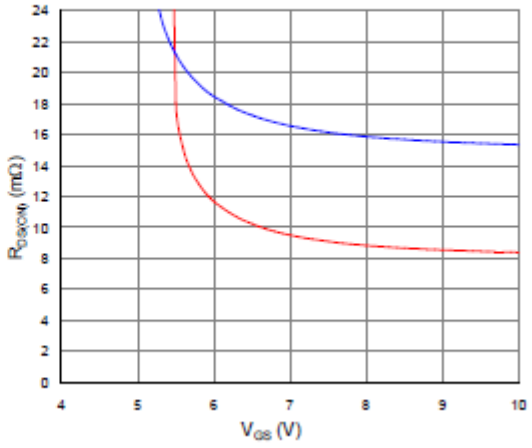


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

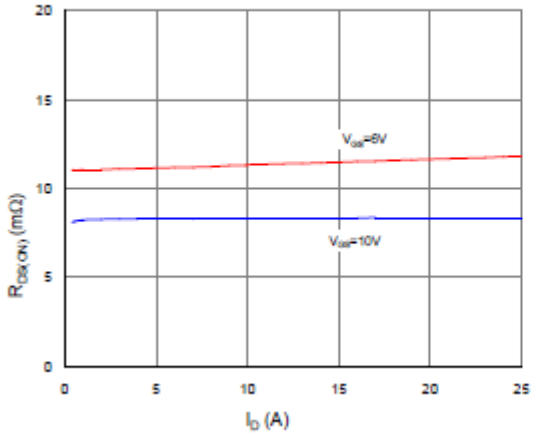


Figure 4. Normalized On-Resistance vs. Junction Temperature

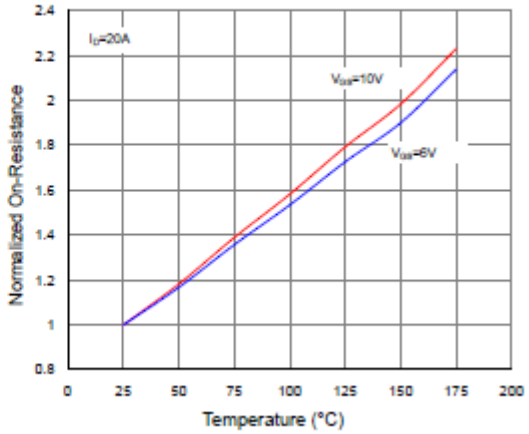


Figure 5. Typical Transfer Characteristics

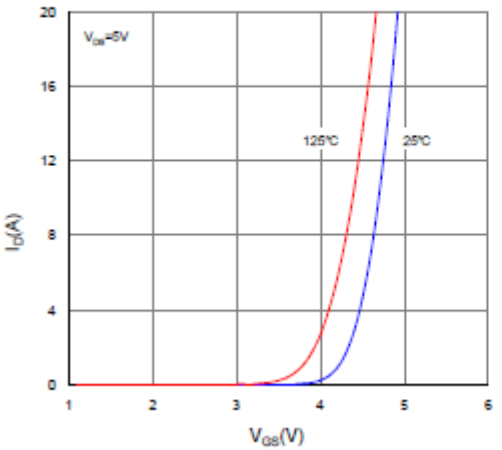
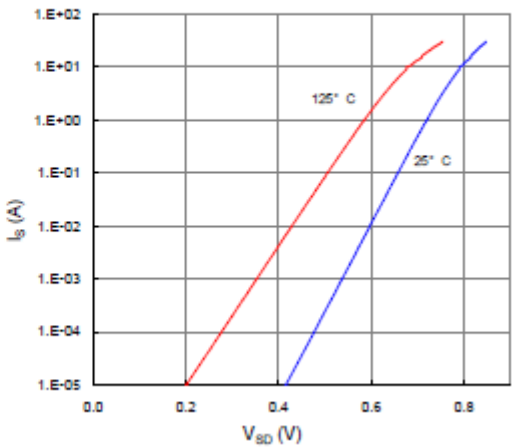


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

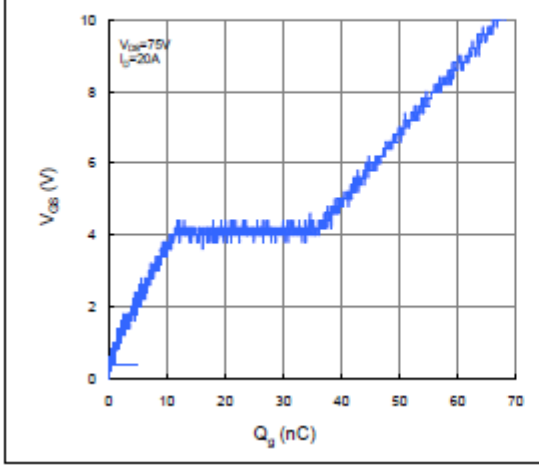


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

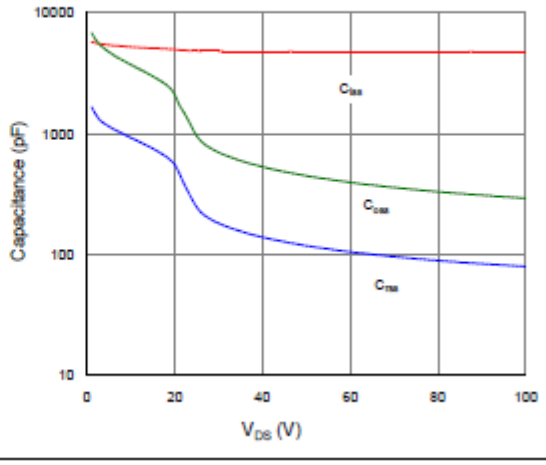


Figure 9. Maximum Safe Operating Area

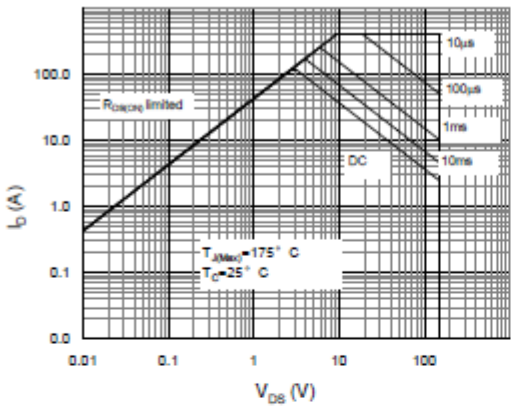


Figure 10. Maximun Drain Current vs. Case Temperature

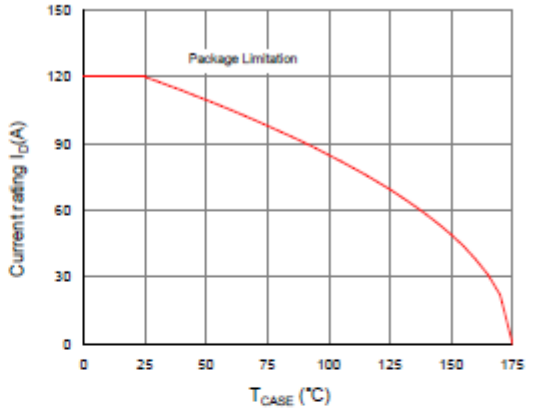
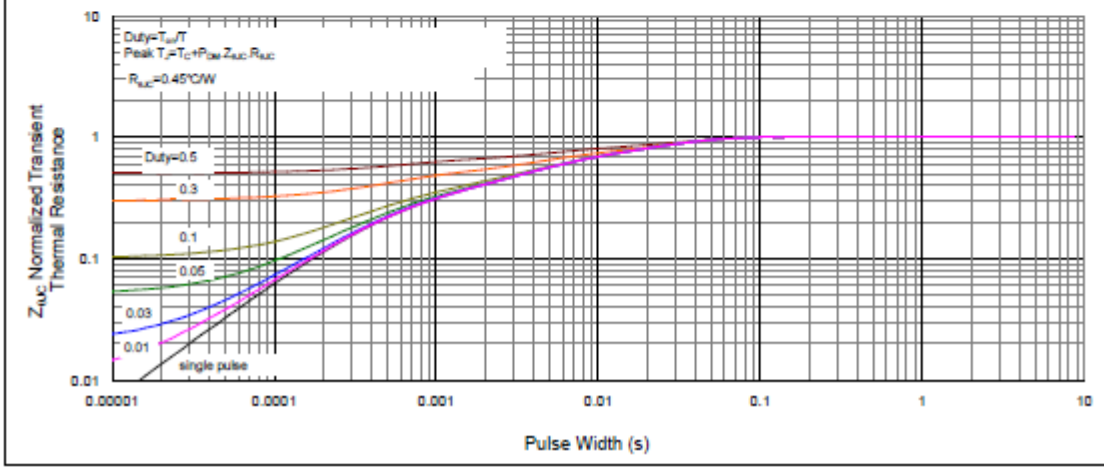
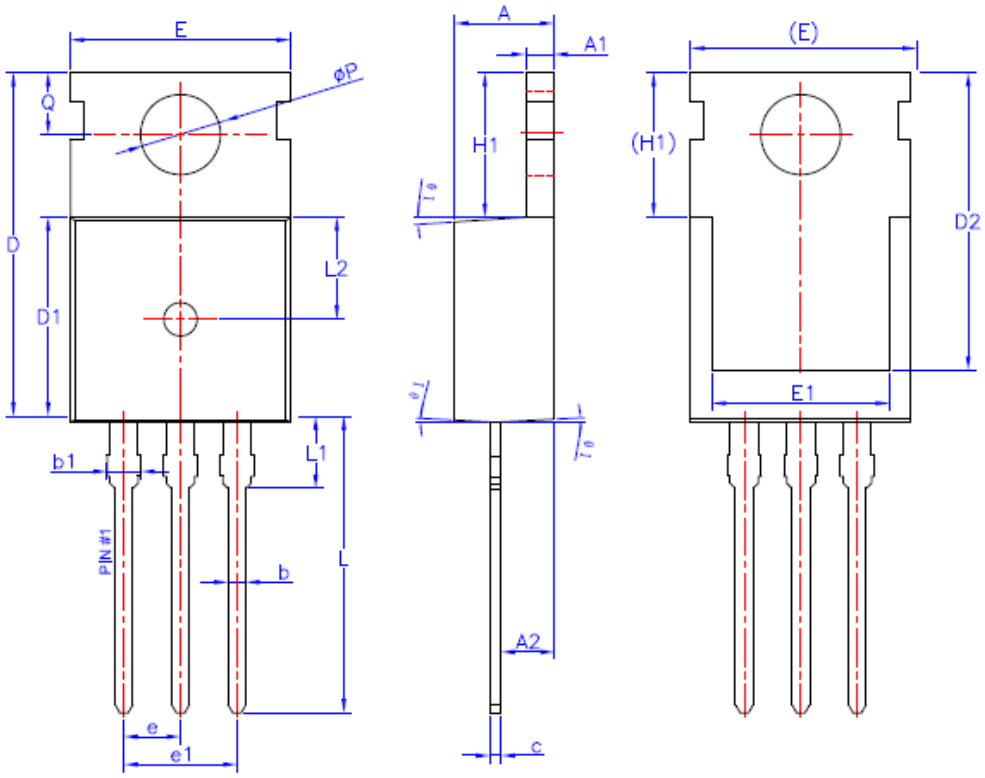


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



TO-220 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	–	0.90
b1	1.42	–	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	–	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	–	–	3.50
L2	4.60REF		
øP	3.55	3.60	3.65
Q	2.73	–	2.87
θ1	1°	3°	5°

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