



# SPN180T10

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN180T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

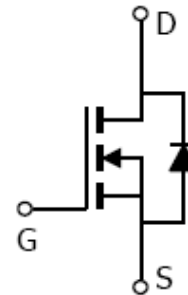
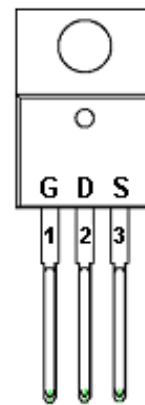
- ◆ 100V/180A,  $R_{DS(ON)}=3.7m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220 package design

### APPLICATIONS

- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

### PIN CONFIGURATION

TO-220



### PART MARKING



A : Lot Code  
B : Date Code  
(YY/MM/DD)



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN180T10T220TGB	TO-220-3L	SPN180T10

※ SPN180T10T220TGB : Tube ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	180	A
		TA=70°C	135	
Pulsed Drain Current	I <sub>DM</sub>	400	A	
Avalanche Energy, Single Pulse @ L=0.1mH, TA=25°C	E <sub>AS</sub>	180	mJ	
Power Dissipation @ TA=25°C	P <sub>D</sub>	166	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	62	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$			1	uA
		$V_{DS}=100V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		3.4	3.7	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		90		S
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$			1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=50V, V_{GS}=10V$ $I_D=20A$		118		nC
Gate-Source Charge	$Q_{gs}$			27		
Gate-Drain Charge	$Q_{gd}$			21		
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V$ $f=1MHz$		7300		pF
Output Capacitance	$C_{oss}$			580		
Reverse Transfer Capacitance	$C_{rss}$			18		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V$ $I_D=20A, R_G=10\Omega$		35		nS
	$t_r$			56		
Turn-Off Time	$t_{d(off)}$			92		
	$t_f$			26		



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## TYPICAL CHARACTERISTICS

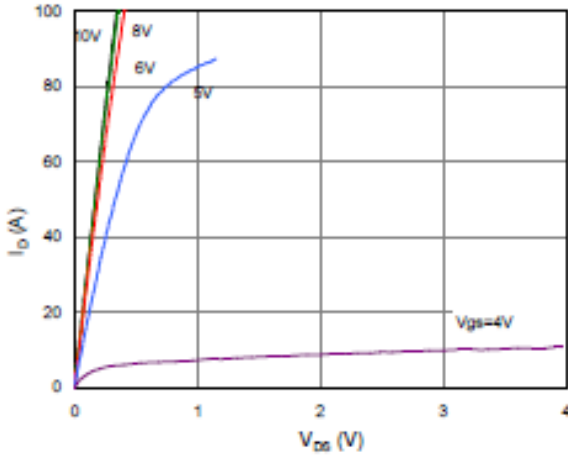


Fig. 1 Output Characteristics

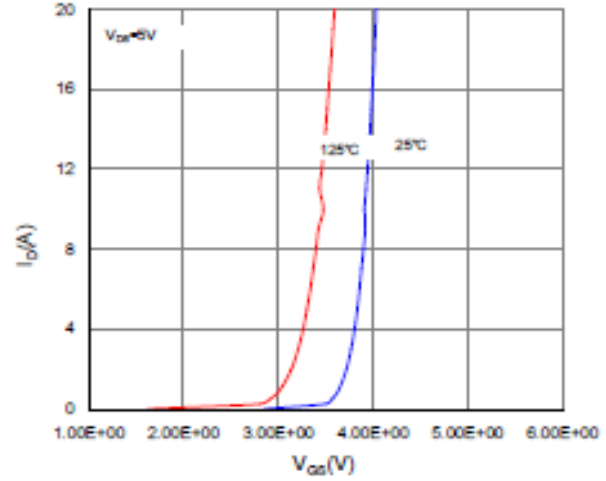


Fig. 2 Transfer Characteristics

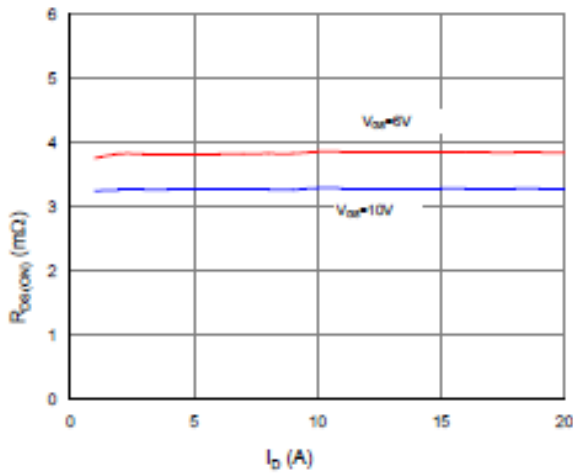


Fig. 3 On Resistances vs Drain Current

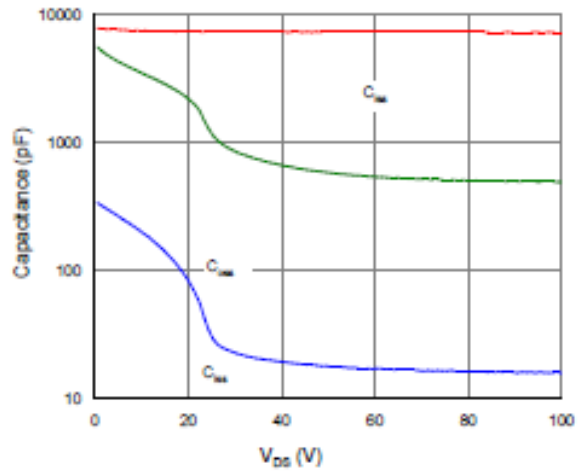


Fig. 4 Capacitance

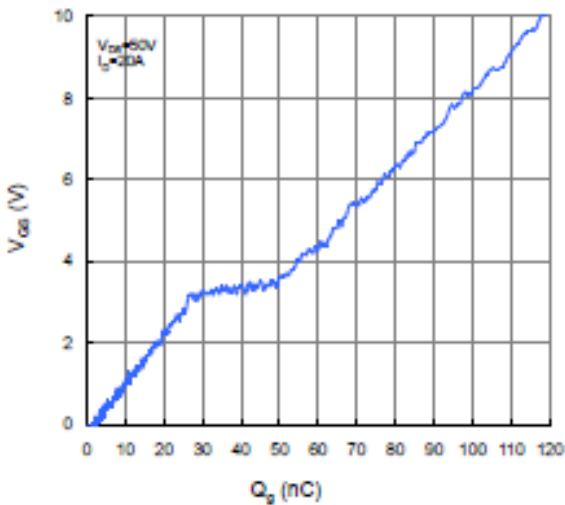


Fig. 5 Gate Charge

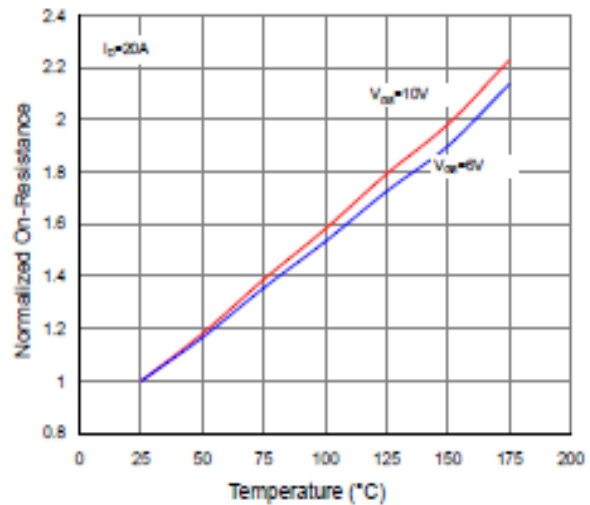


Fig. 6 On-Resistance vs Junction Temperature



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### TYPICAL CHARACTERISTICS

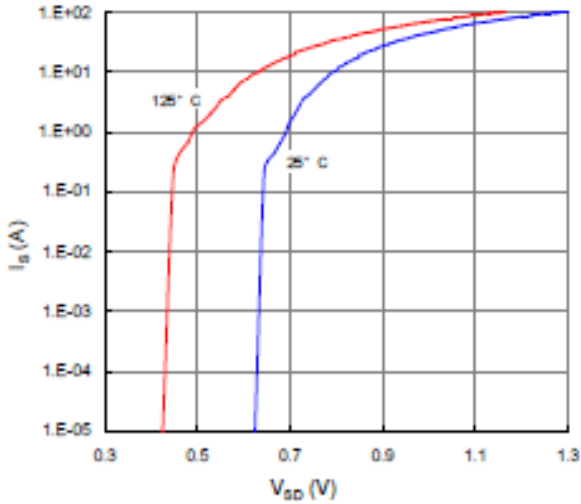


Fig. 7 Source Drain Diode Forward Voltage

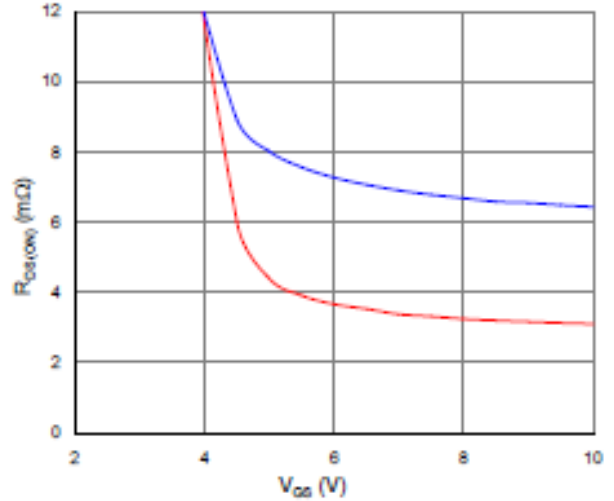


Fig. 8 On Resistance vs Gate Source Voltage

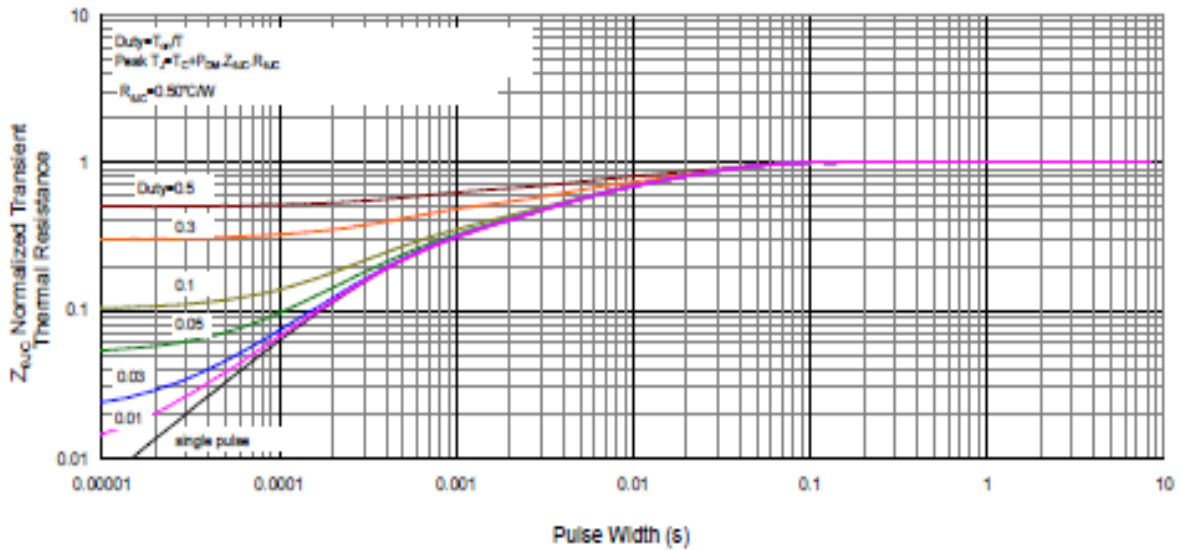


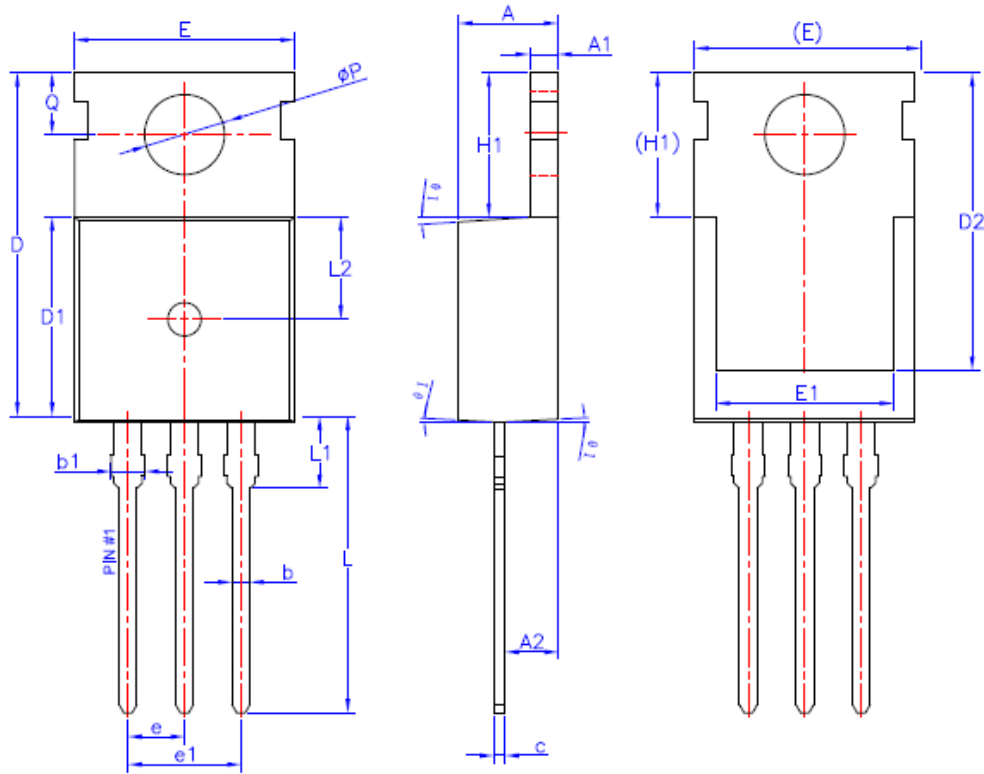
Fig. 9 Normalized Thermal Transient Impedance, Junction to Foot



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### TO-220 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	—	0.90
b1	1.42	—	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	—	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	—	—	3.50
L2	4.60REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	—	2.87
$\theta 1$	1°	3°	5°



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