



# SPN230T06

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN230T06 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

- ◆ 60V/230A,  $R_{DS(ON)}=2.5m\Omega@V_{GS}=10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-220-3L and TO-263-2L package design

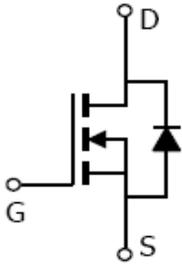
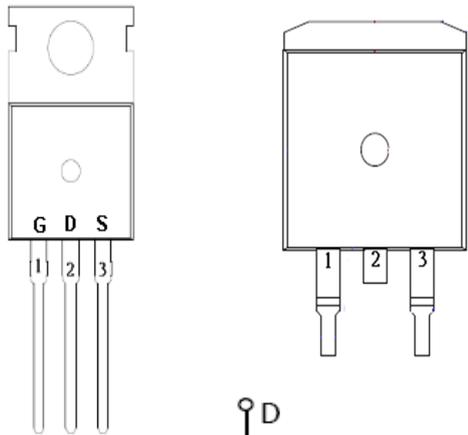
### APPLICATIONS

- AC/DC Synchronous Rectifier
- Load Switch
- UPS
- Power Tool
- Motor Control

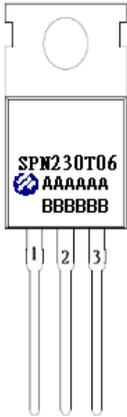
### PIN CONFIGURATION

TO-220-3L

TO-263-2L



### PART MARKING



AAAAA: Wafer lot no  
BBBBBB: date code

A : Lot Code  
B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN230T06T220TGB	TO-220-3L	SPN230T06
SPN230T06T262RGB	TO-263-2L	SPN230T06

※ SPN230T06T220TGB : Tube ; Pb – Free ; Halogen - Free

※ SPN230T06T262RGB : Tape&Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	230
		TA=70°C	160
A			
Pulsed Drain Current	I <sub>DM</sub>	500	A
Avalanche Energy, Single Pulse @ L=1mH, TA=25°C	E <sub>AS</sub>	350	mJ
Power Dissipation @ TA=25°C	P <sub>D</sub>	104	W
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Case	R <sub>θJC</sub>	1.2	°C/W



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	2.8	4.0	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$ $T_J=25^\circ C$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J=100^\circ C$			100	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		2.1	2.5	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=20A$		80		S
Gate Resistance	$R_G$	$V_{GS}=0V, V_{DS}=Open, f=1MHz$		0.7		Ω
Diode Forward Voltage	$V_{SD}$	$I_S=20A, V_{GS}=0V$		0.9	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=30V, V_{GS}=10V$ $I_D=20A$		85		nC
Gate-Source Charge	$Q_{gs}$			24		
Gate-Drain Charge	$Q_{gd}$			14		
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V$ $f=1MHz$		7070		pF
Output Capacitance	$C_{oss}$			2140		
Reverse Transfer Capacitance	$C_{rss}$			63		
Turn-On Time	$t_{d(on)}$	$V_{DD}=30V, V_{GS}=10V$ $I_D=20A, R_G=10\Omega$		36		nS
	$t_r$			62		
Turn-Off Time	$t_{d(off)}$			95		
	$t_f$			34		



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### TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

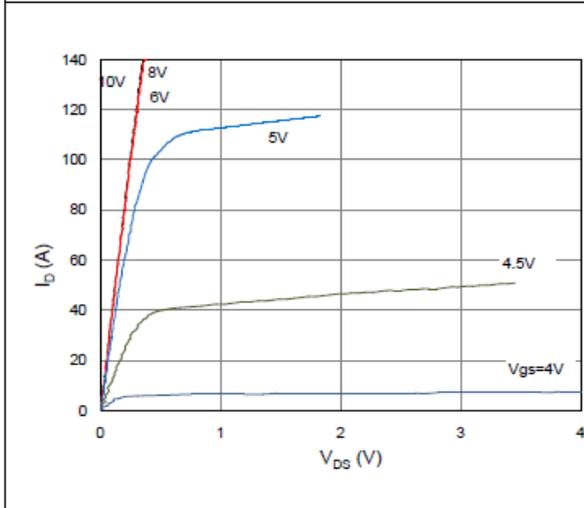


Figure 2. On-Resistance vs. Gate-Source Voltage

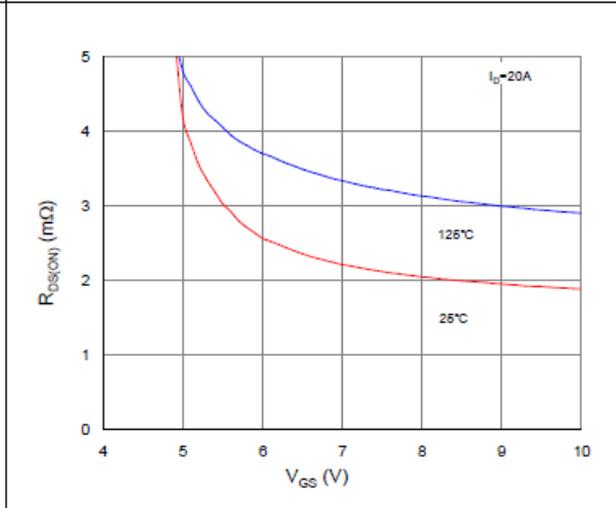


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

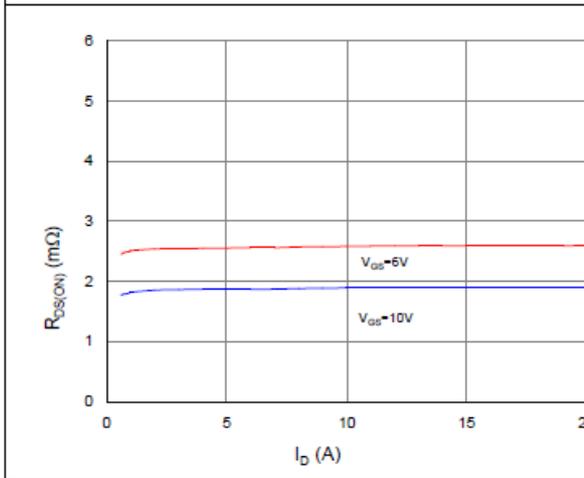


Figure 4. Normalized On-Resistance vs. Junction Temperature

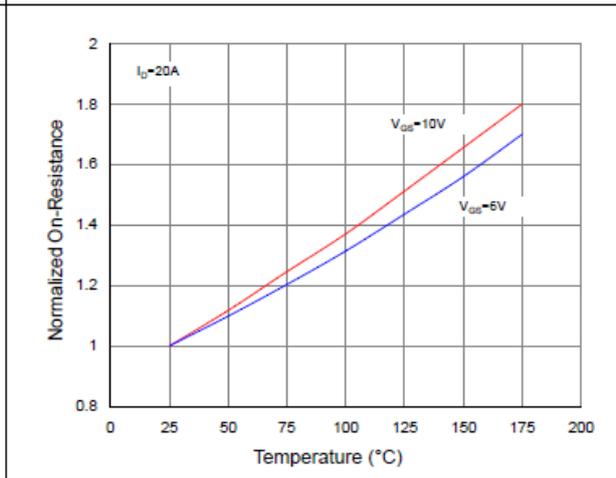


Figure 5. Typical Transfer Characteristics

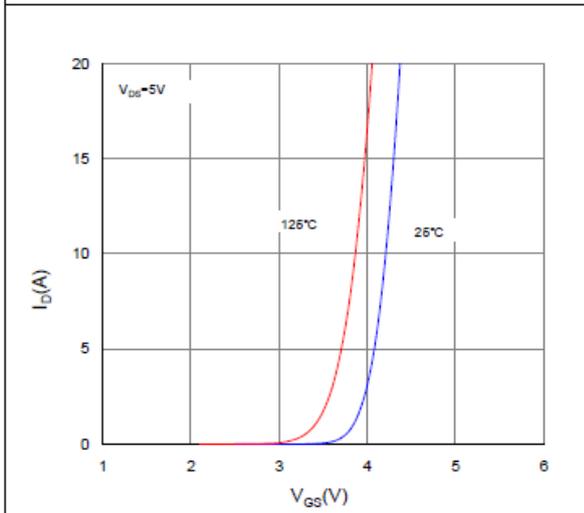
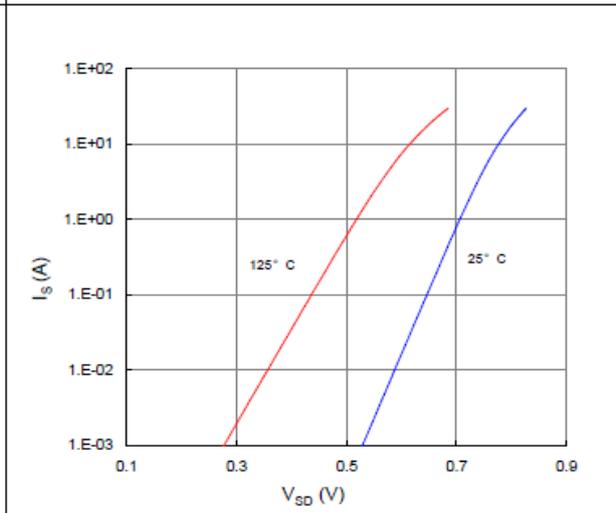


Figure 6. Typical Source-Drain Diode Forward Voltage





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### TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

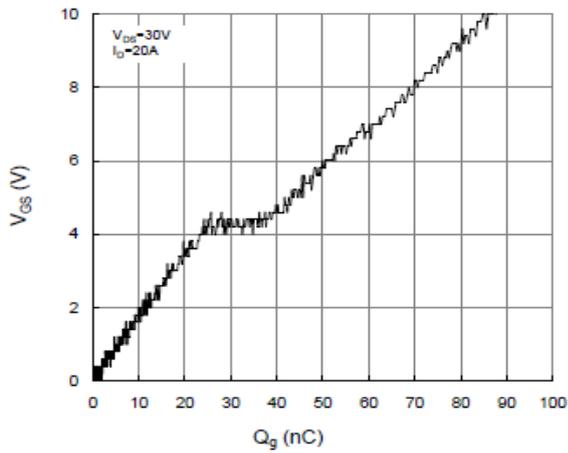


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

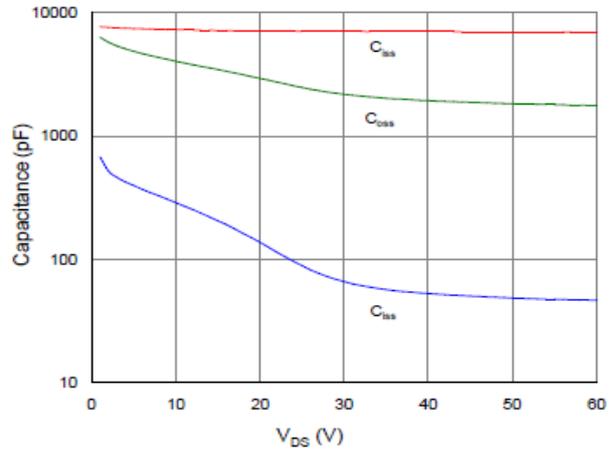


Figure 9. Maximum Safe Operating Area

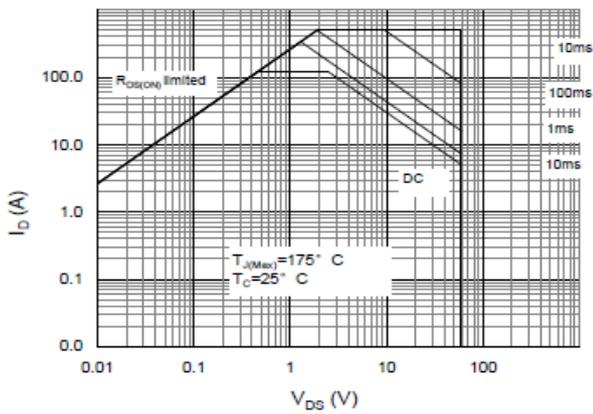


Figure 10. Maximum Drain Current vs. Case Temperature

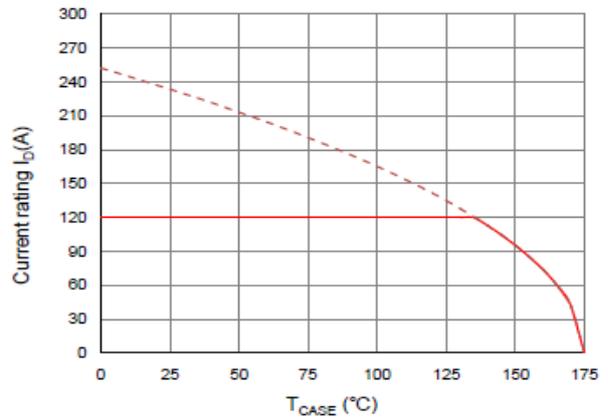
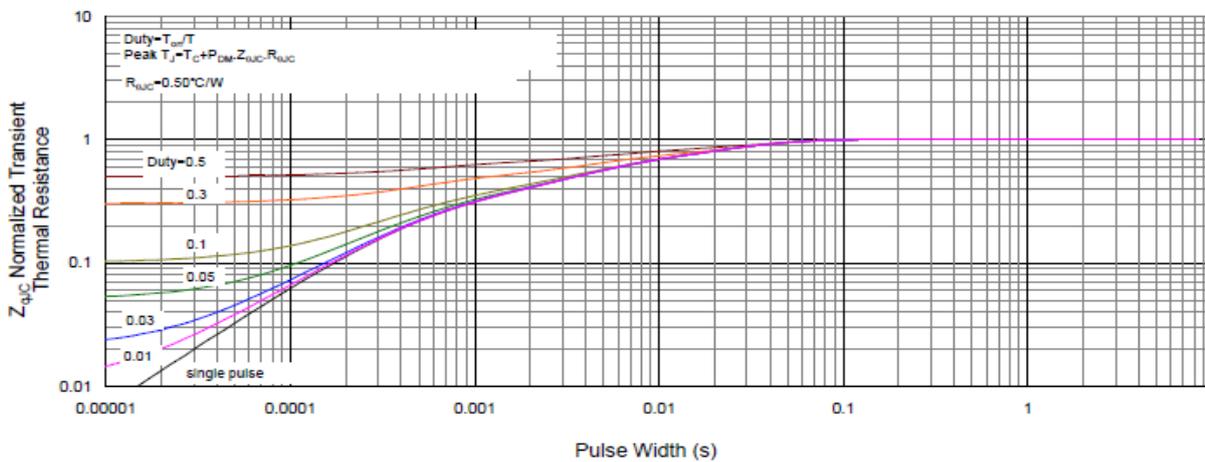


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

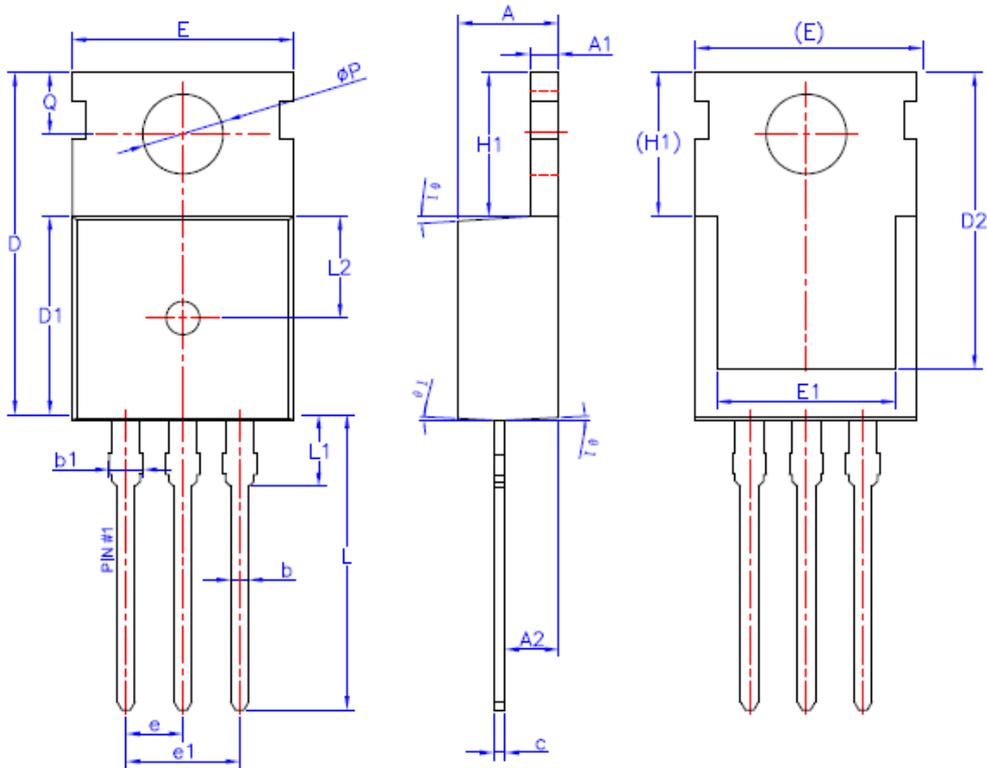




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## N-Channel Enhancement Mode MOSFET

### TO-220-3L PACKAGE OUTLINE



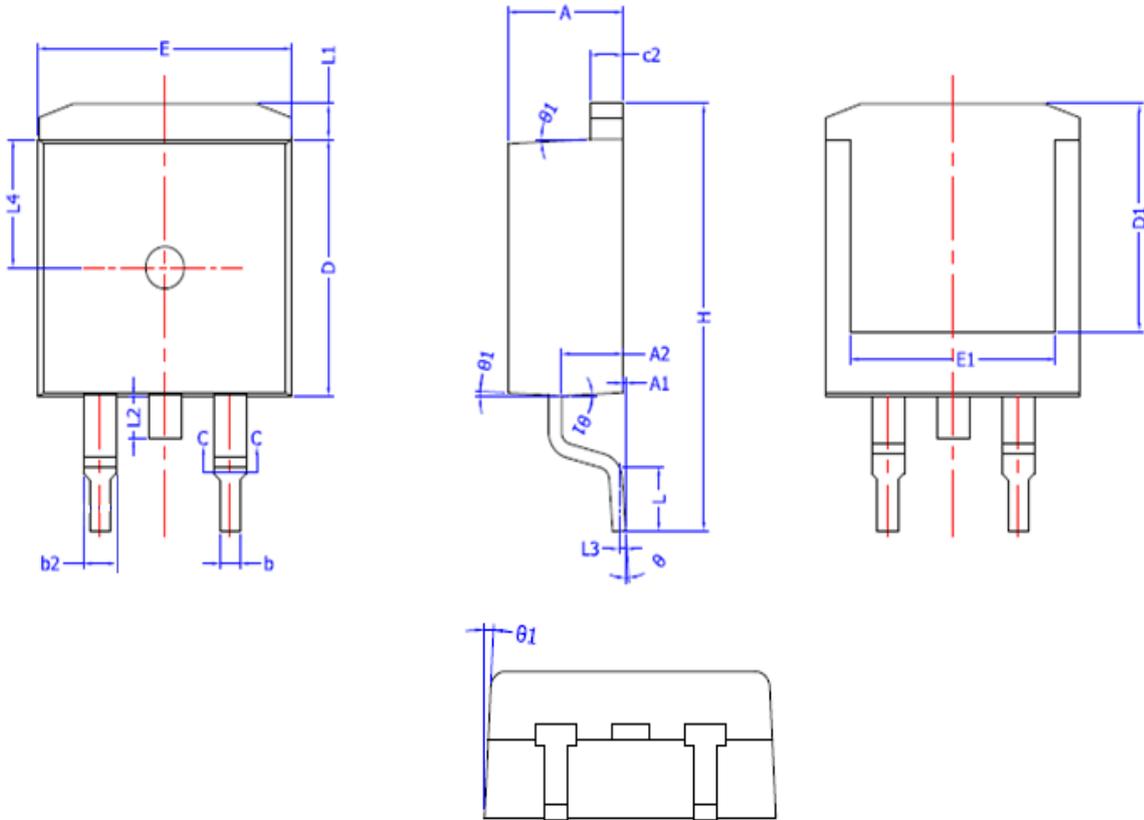
SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	0.60	0.90
b1	-	-	1.40
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	-	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	-	-	3.50
L2	4.6REF		
$\phi P$	3.55	3.60	3.65
Q	2.73	-	2.87
$\theta 1$	1°	3°	5°



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### TO-263-2L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	0.00	0.10	0.25
A2	2.20	2.40	2.60
b	0.71	-	0.91
b2	1.17	--	1.37
c	0.47	--	0.60
c2	1.25	1.30	1.35
D	9.10	9.20	9.30
D1	8.00	--	--
E	9.80	9.90	10.00
E1	7.80	--	--
e	2.54BSC		
H	14.90	15.30	15.70
L	2.00	2.30	2.60
L1	1.12	1.27	1.42
L2	--	--	1.75
L3	0.25BSC		
L4	4.60 REF		
$\theta$	0°	--	8°
$\theta 1$	1°	3°	5°



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