



SPN2324

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2324 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN2324 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

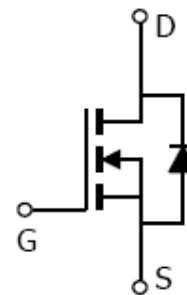
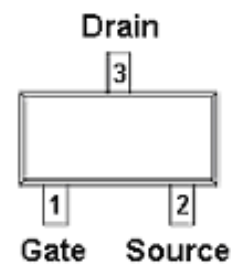
APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch

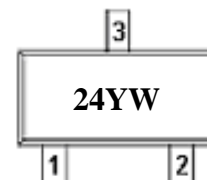
FEATURES

- ◆ 100V/1A, $R_{DS(ON)} = 310m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

PIN CONFIGURATION(SOT-23)



PART MARKING



YW: Date Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2324S23RGB	SOT-23	24YW

※ SPN2324S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	100	V	
Gate –Source Voltage	V _{GSS}	±30	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	3.0	A
		TA=70°C	2.0	
Pulsed Drain Current	I _{DM}	10	A	
Power Dissipation	P _D	TA=25°C	1.25	W
		TA=70°C	0.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W	



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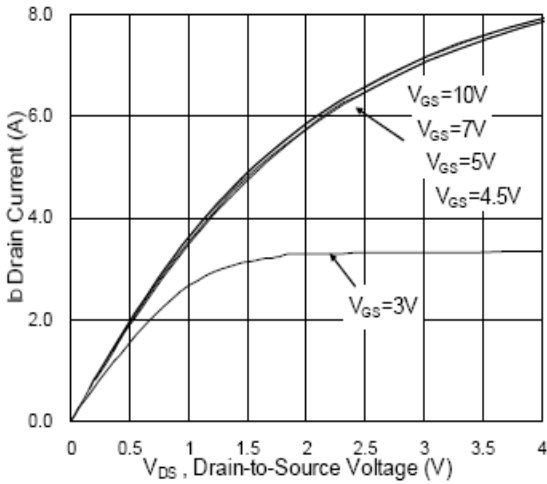
ELECTRICAL CHARACTERISTICS (T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V			1	μA
		V _{DS} =80V, V _{GS} =0V T _J =125°C			5	
On-State Drain Current	I _{D(on)}	V _{DS} ≥5V, V _{GS} =10V	3.0			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3A		0.26	0.31	Ω
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =3A		2.4		S
Diode Forward Voltage	V _{SD}	I _S =1A, V _{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =80V, V _{GS} =10V I _D =5A		9	13	nC
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			1.4		
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V f=1MHz		508		pF
Output Capacitance	C _{oss}			29		
Reverse Transfer Capacitance	C _{rss}			16.5		
Turn-On Time	t _{d(on)}	V _{DD} =50V, R _L =10Ω I _D =3A, V _{GEN} =10V R _G =3.3Ω		2		nS
	t _r			21.5		
Turn-Off Time	t _{d(off)}			11.2		
	t _f			18.8		

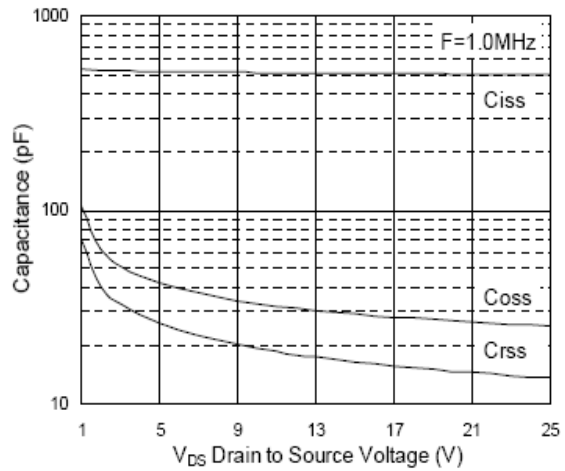


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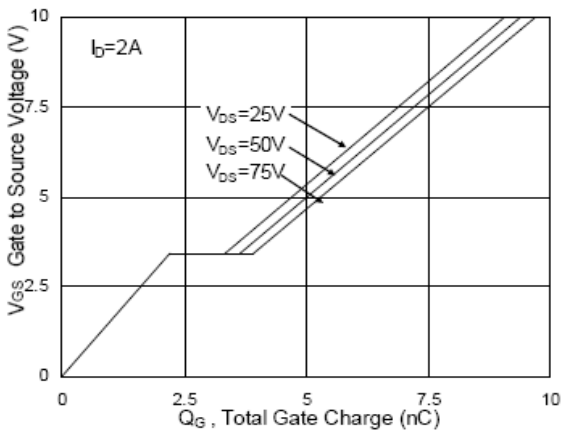
TYPICAL CHARACTERISTICS



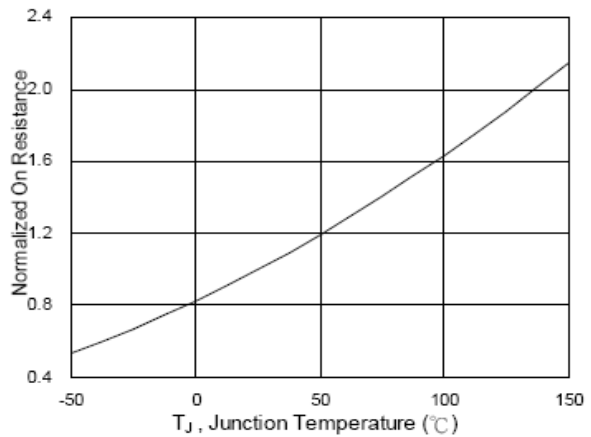
Output Characteristics



Capacitance



Gate Charge



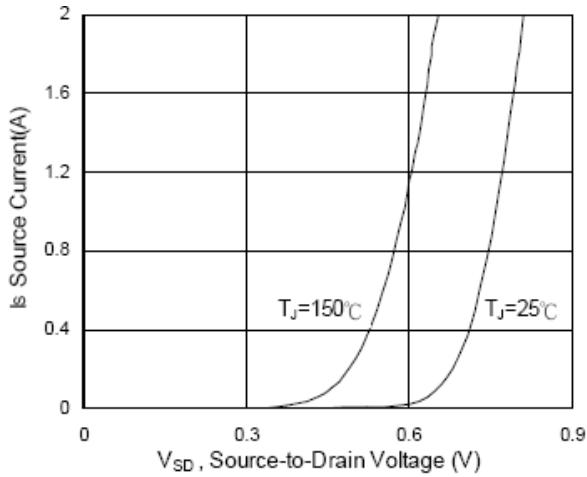
On-Resistance vs. Junction Temperature



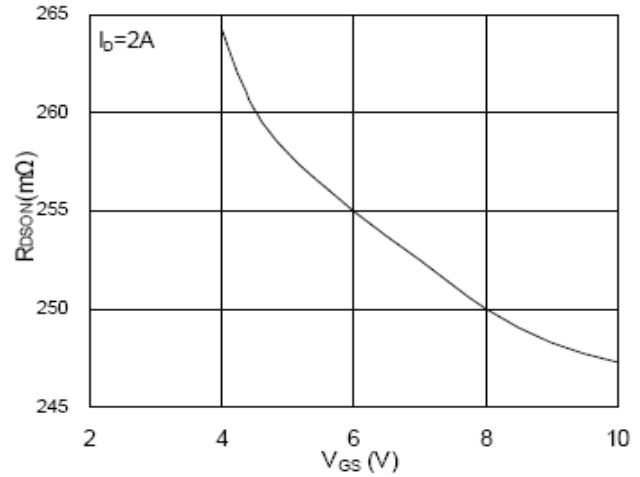
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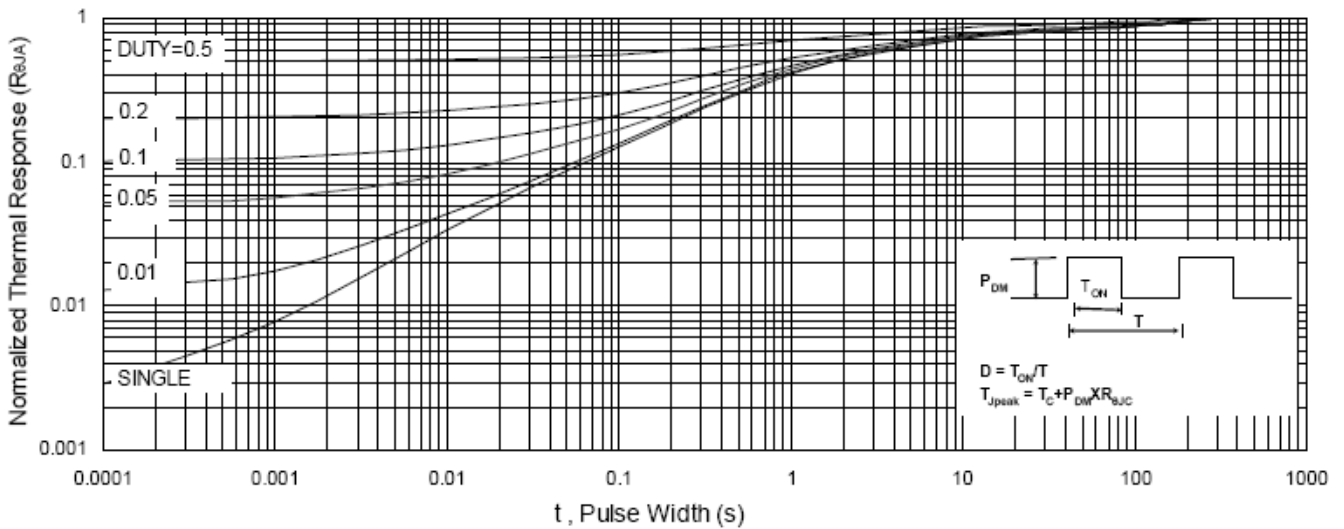
TYPICAL CHARACTERISTICS



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-Source Voltage



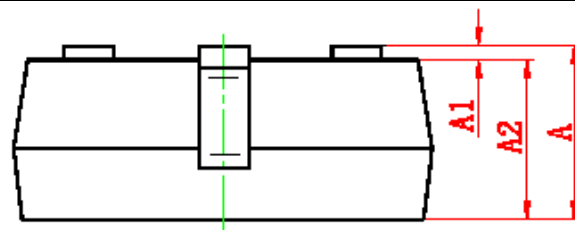
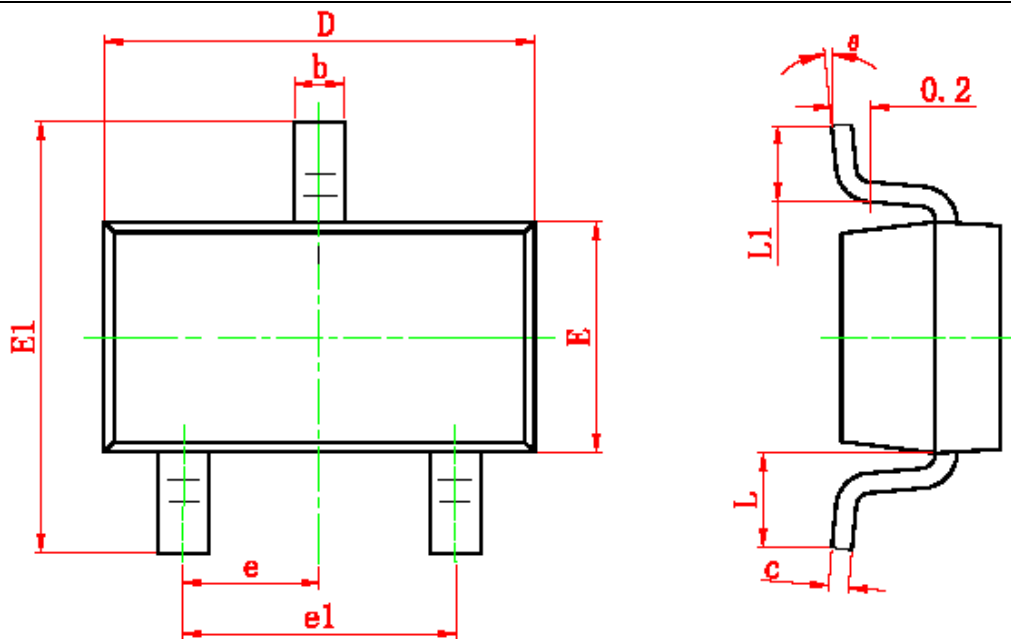
Normalized Thermal Transient Impedance, Junction to Foot



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SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	6°



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