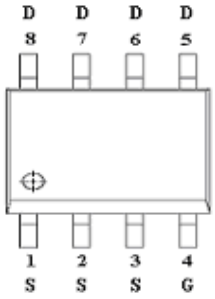
SPN4402W
N-Channel Enhancement Mode MOSFET

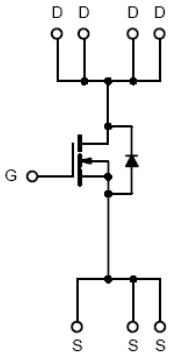
DESCRIPTION
The SPN4402W is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

FEATURES
- 30V/12A,$R_{DS(ON)}$= 15mΩ@V_{GS}= 10V
- 30V/10A,$R_{DS(ON)}$= 18mΩ@V_{GS}= 4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOP – 8P package design

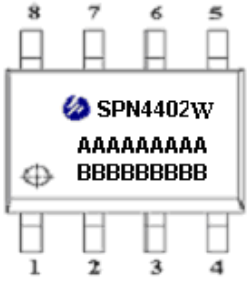
APPLICATIONS
- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)





PART MARKING



A : Lot Code
B : Date Code

SPN4402W
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4402WS8RGB	SOP- 8P	SPN4402W

※ SPN4402WS8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

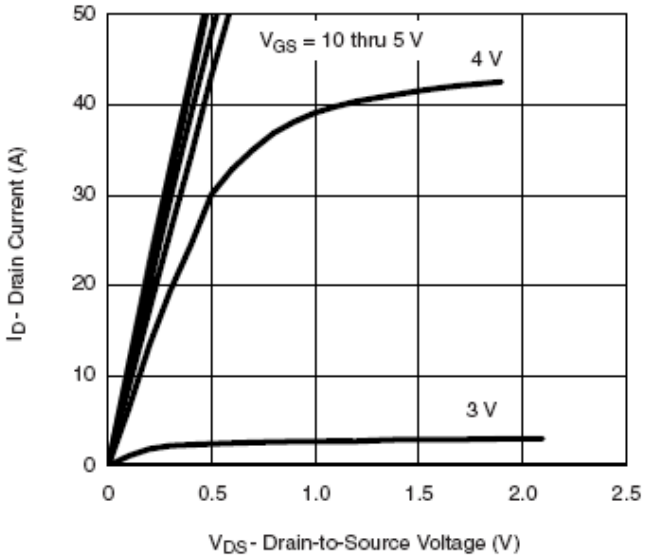
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	12	A
	T_A=70℃		10	
Pulsed Drain Current		I_{DM}	30	A
Continuous Source Current(Diode Conduction)		I_S	2.3	A
Power Dissipation	T_A=25℃	P_D	2.5	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	80	℃/W

ELECTRICAL CHARACTERISTICS

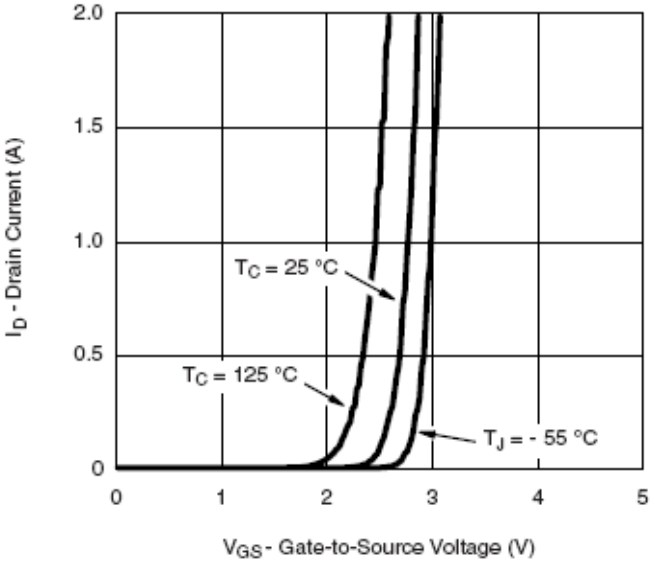
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.6		1.8	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V			1	uA
		V_{DS}=24V,V_{GS}=0V T_J=55℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V	25			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=12A		0.010	0.015	Ω
		V_{GS}=4.5V,I_D=10A		0.013	0.018	
Forward Transconductance	gfs	V_{DS}=15V,I_D=6.2A		13		S
Diode Forward Voltage	V_{SD}	I_S=2.3A,V_{GS} =0V		0.5	1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V,V_{GS}=10V I_D= 2A		10	18	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			2.0		
Input Capacitance	C_{iss}	V_{DS}=15VV_{GS}=0V f=1MHz		850		pF
Output Capacitance	C_{oss}			158		
Reverse Transfer Capacitance	C_{rss}			120		
Turn-On Time	$t_{d(on)}$	V_{DD}=15V,R_L=15Ω I_D≡5.0A,V_{GEN}=10V R_G=1Ω		10	15	nS
	t_r			4	12	
Turn-Off Time	$t_{d(off)}$			15	30	
	t_f			10	15	

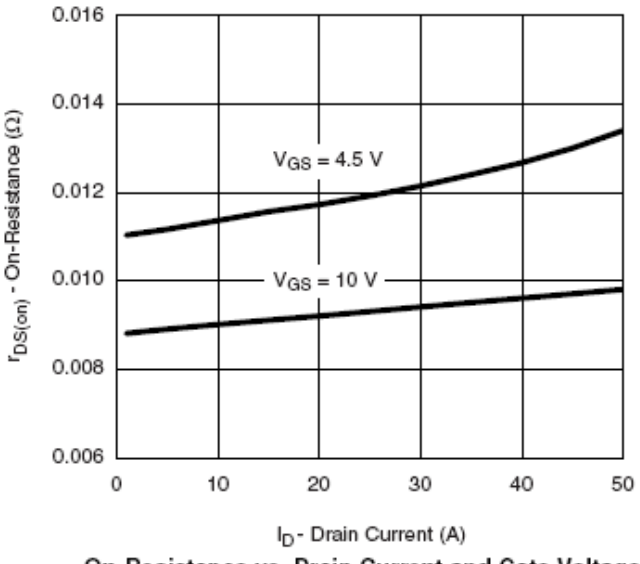
TYPICAL CHARACTERISTICS



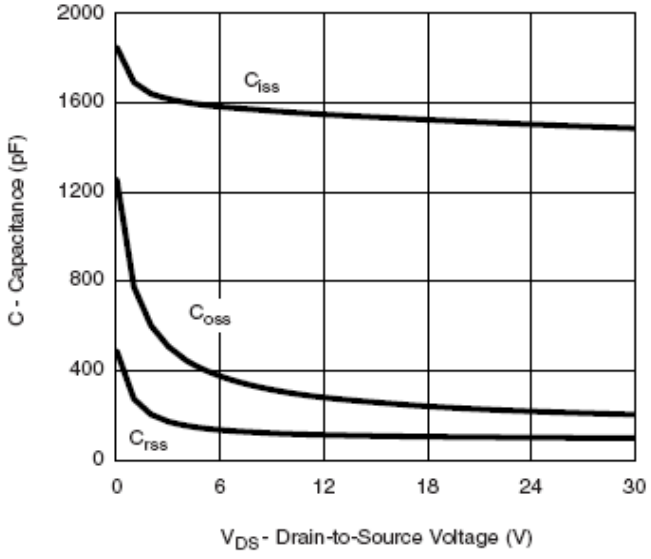
Output Characteristics



Transfer Characteristics

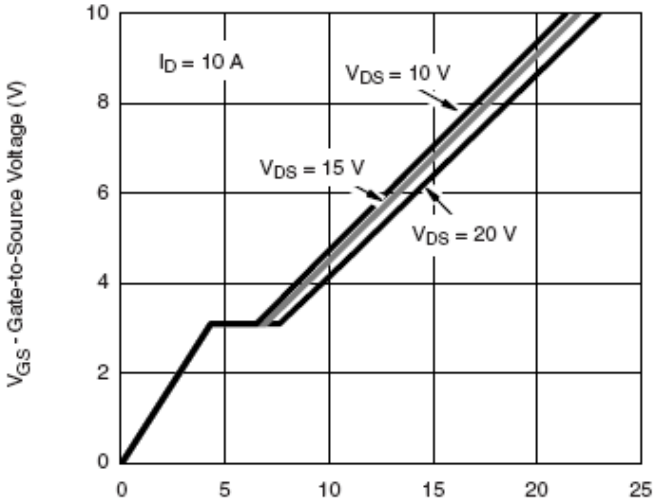


On-Resistance vs. Drain Current and Gate Voltage

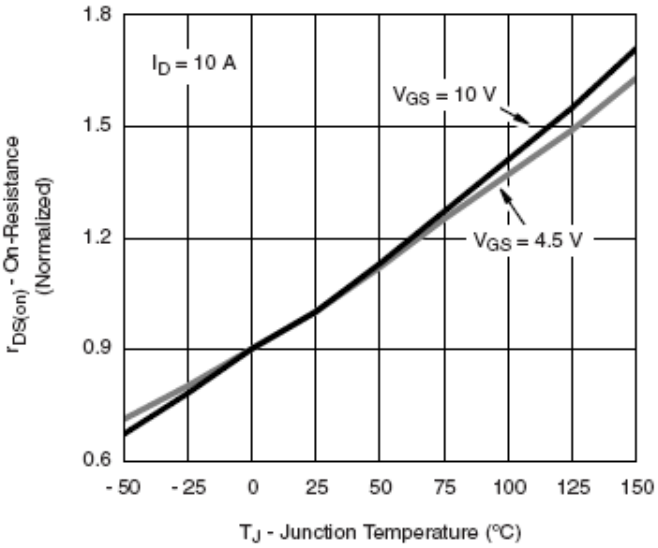


Capacitance

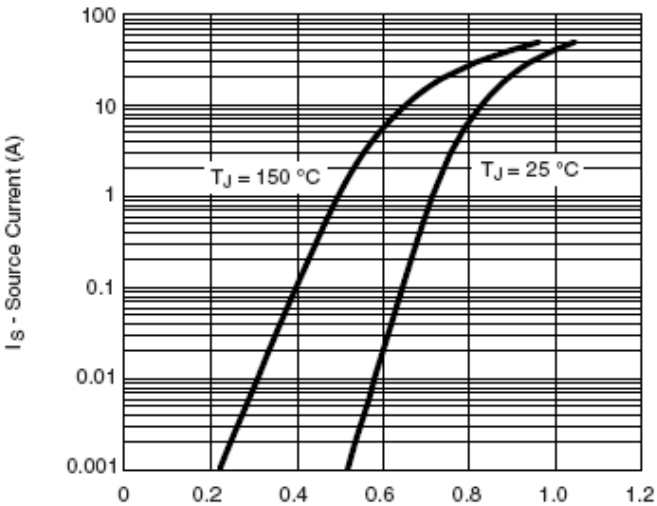
TYPICAL CHARACTERISTICS



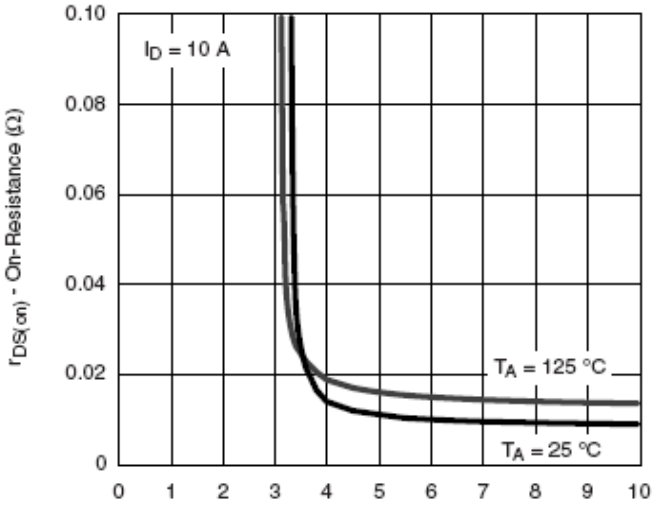
Gate Charge



On-Resistance vs. Junction Temperature

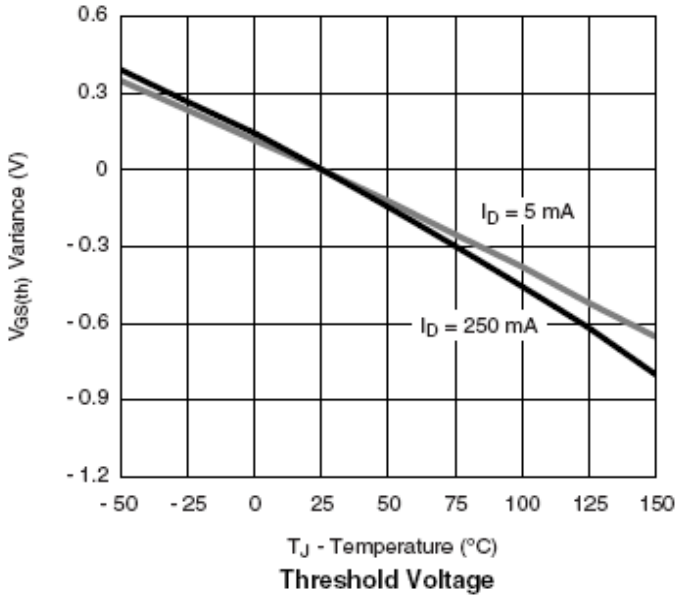


Source-Drain Diode Forward Voltage

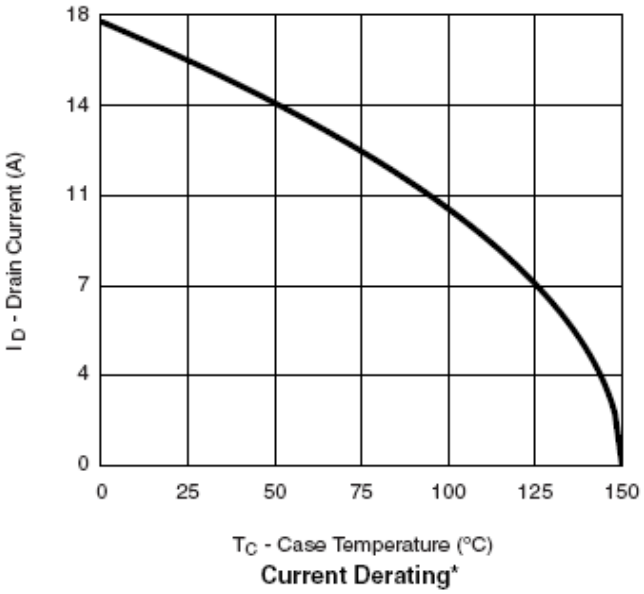


On-Resistance vs. Gate-to-Source Voltage

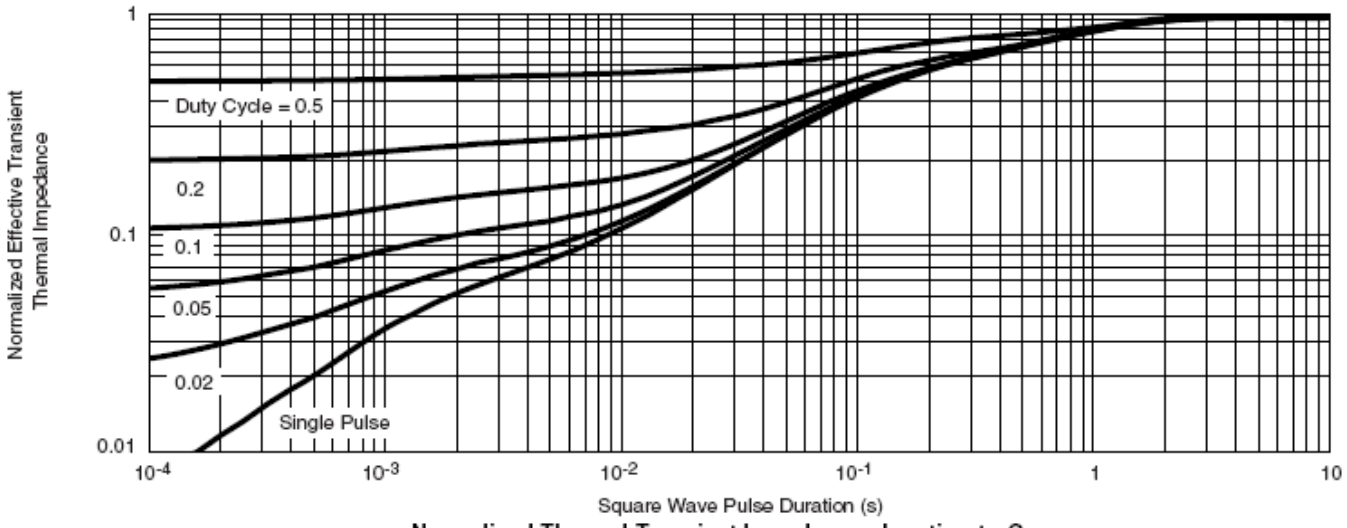
TYPICAL CHARACTERISTICS



Threshold Voltage

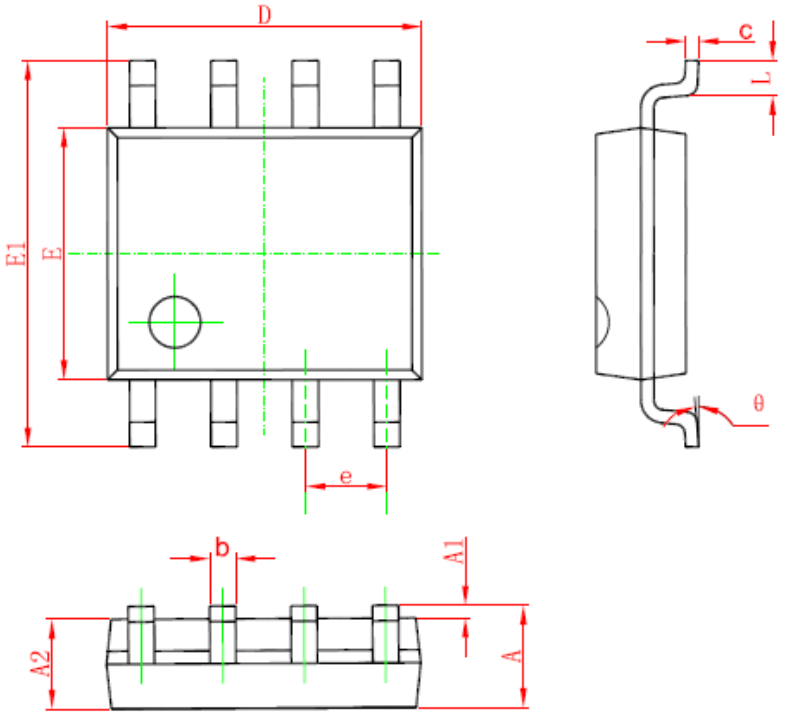


Current Derating*



Normalized Thermal Transient Impedance, Junction-to-Case

SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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