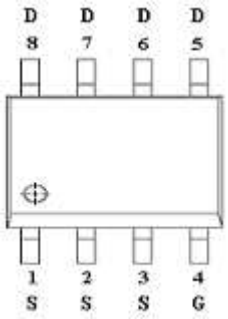
SPN4428
N-Channel Enhancement Mode MOSFET

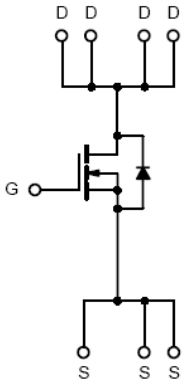
DESCRIPTION
The SPN4428 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

FEATURES
- 20V/14A,$R_{DS(ON)}$= 20mΩ@V_{GS}= 4.5V
- 20V/7.0A,$R_{DS(ON)}$= 28mΩ@V_{GS}= 2.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOP – 8P package design

APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)





PART MARKING

A : Lot Code
B : Date Code

SPN4428
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4428S8RGB	SOP- 8P	SPN4428

※ SPN4428S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	9	A
	T_A=70℃		5.6	
Pulsed Drain Current		I_{DM}	30	A
Continuous Source Current(Diode Conduction)		I_S	2.3	A
Power Dissipation	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	80	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	0.5		1.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±16V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0V			1	uA
		V_{DS}=16V,V_{GS}=0V T_J=85℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V	25			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 4.5V,I_D=14A		0.016	0.020	Ω
		V_{GS}=2.5V,I_D=7.0A		0.022	0.028	
Forward Transconductance	gfs	V_{DS}=15V,I_D=6.2A		30		S
Diode Forward Voltage	V_{SD}	I_S=2.3A,V_{GS} =0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V, V_{GS}=4.5V I_D= 14A		9.8		nC
Gate-Source Charge	Q_{gs}			2.1		
Gate-Drain Charge	Q_{gd}			3		
Input Capacitance	C_{iss}	V_{DS}=15, V_{GS}=0V f=1MHz		772		pF
Output Capacitance	C_{oss}			83		
Reverse Transfer Capacitance	C_{rss}			79		
Turn-On Time	$t_{d(on)}$	V_{DD}=10V, I_D≡14A, V_{GS}=4.5V, R_G=3.3Ω		4		nS
	t_r			12.5		
Turn-Off Time	$t_{d(off)}$			20		
	t_f			8		

TYPICAL CHARACTERISTICS

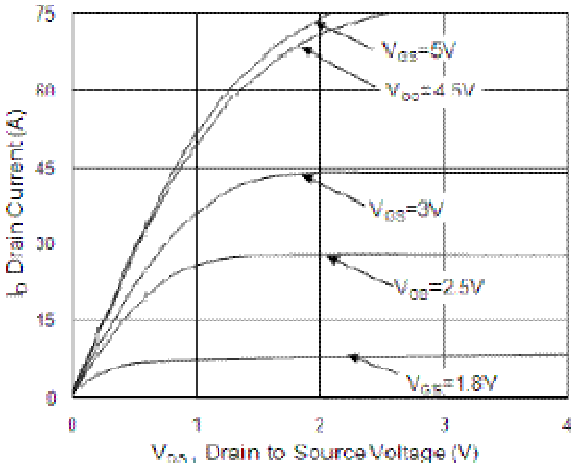


Fig. 1 Typical Output Characteristics

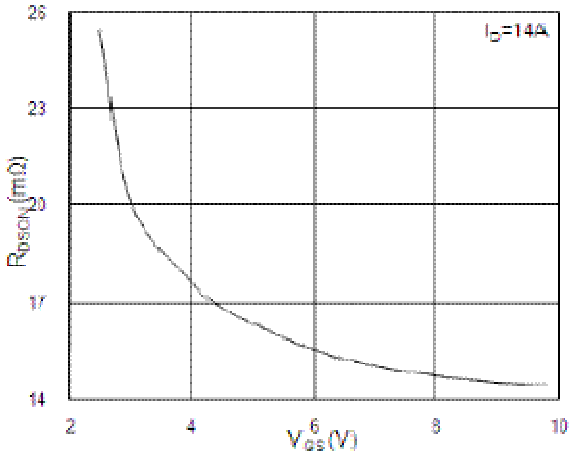


Fig. 2 On-Resistance vs Gate Voltage

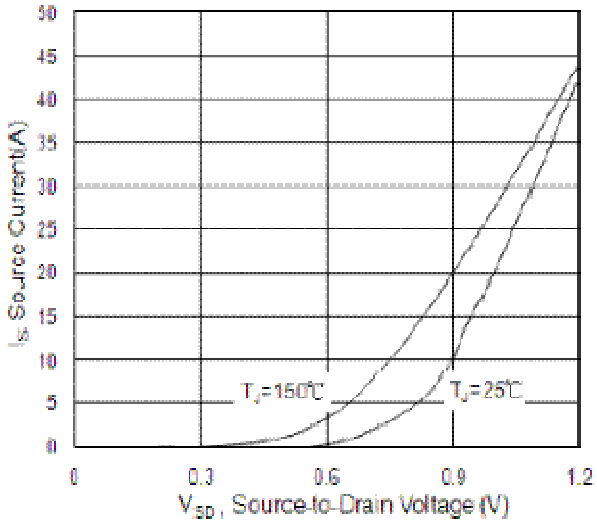


Fig. 3 Forward Characteristics

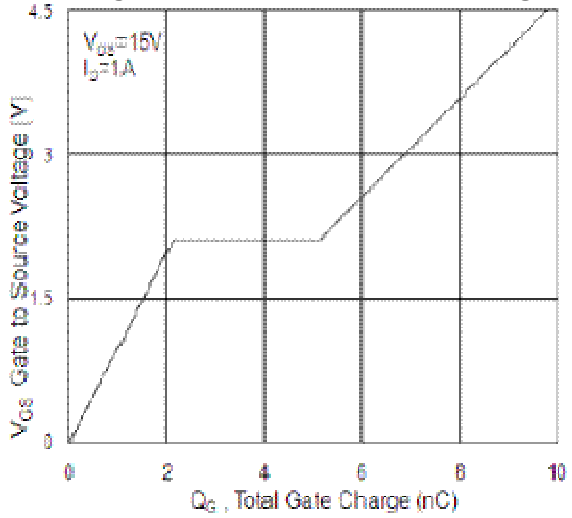


Fig. 4 Total Gate Charge

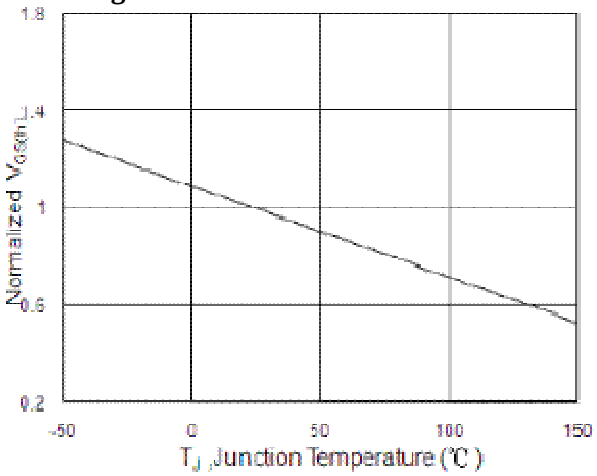


Fig. 5 Vgs vs Temperature

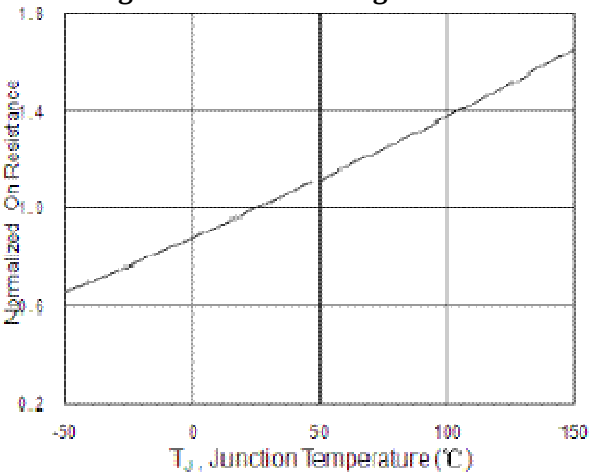


Fig. 6 Rdson vs Temperature

TYPICAL CHARACTERISTICS

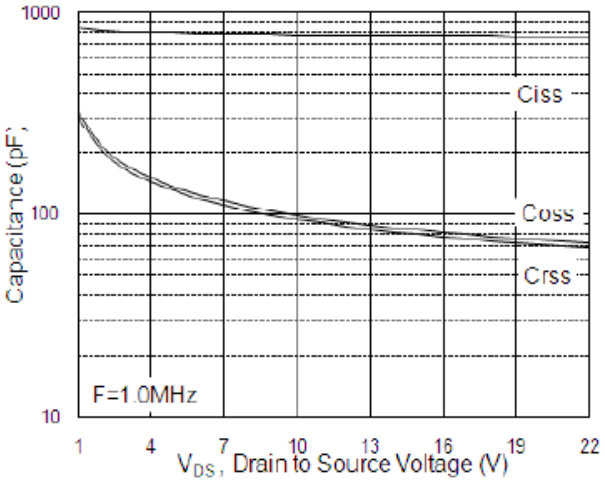


Fig. 7 Capacitance vs Vds

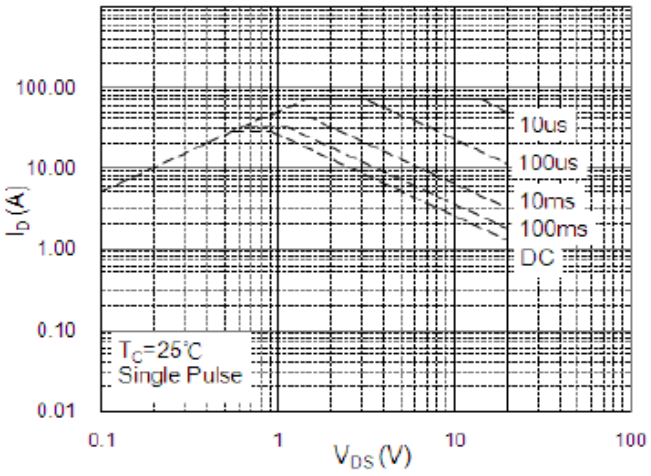


Fig. 8 Safe Operation Region

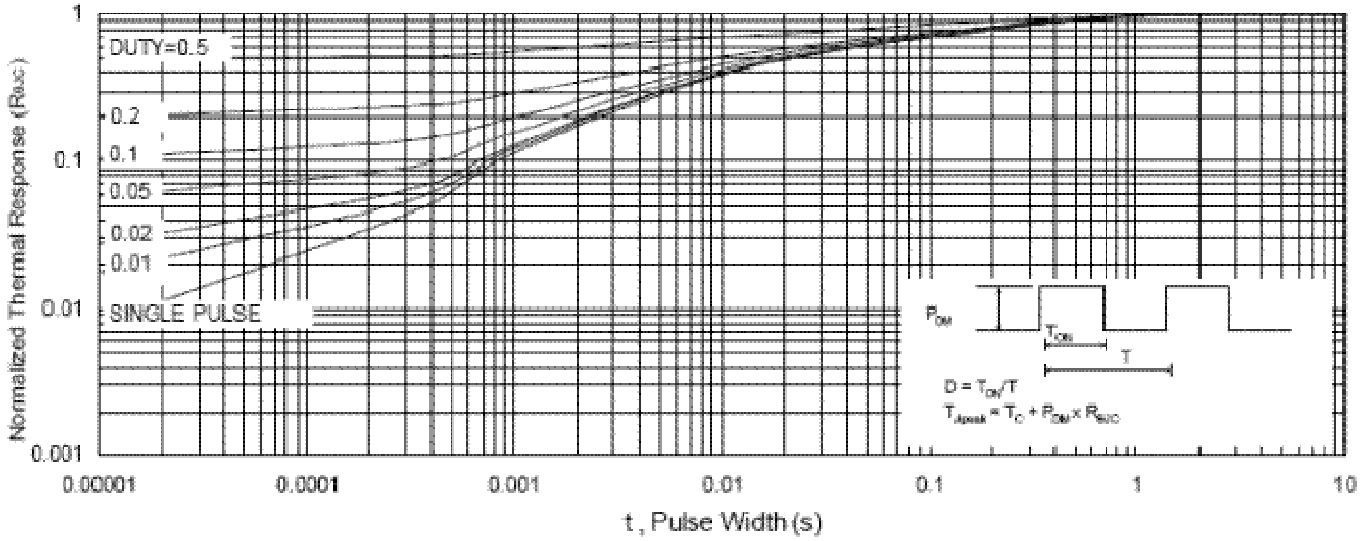


Fig. 9 Maximum Transient Thermal Impedance

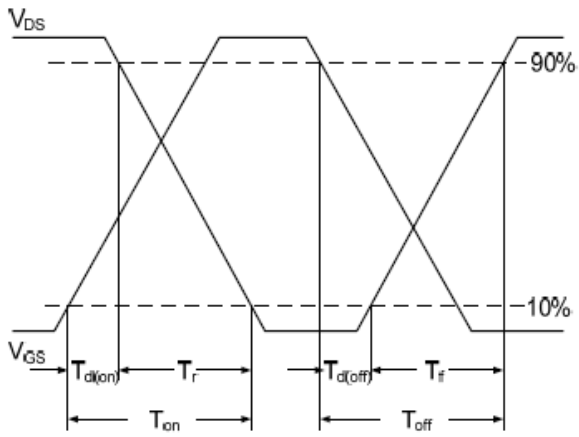


Fig. 10 Switching Time Waveform

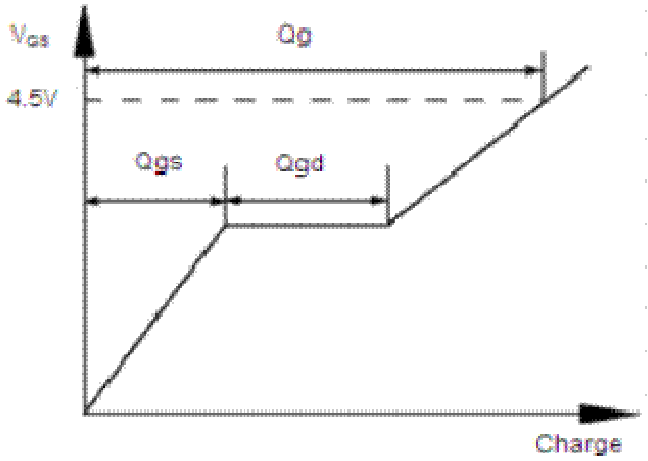
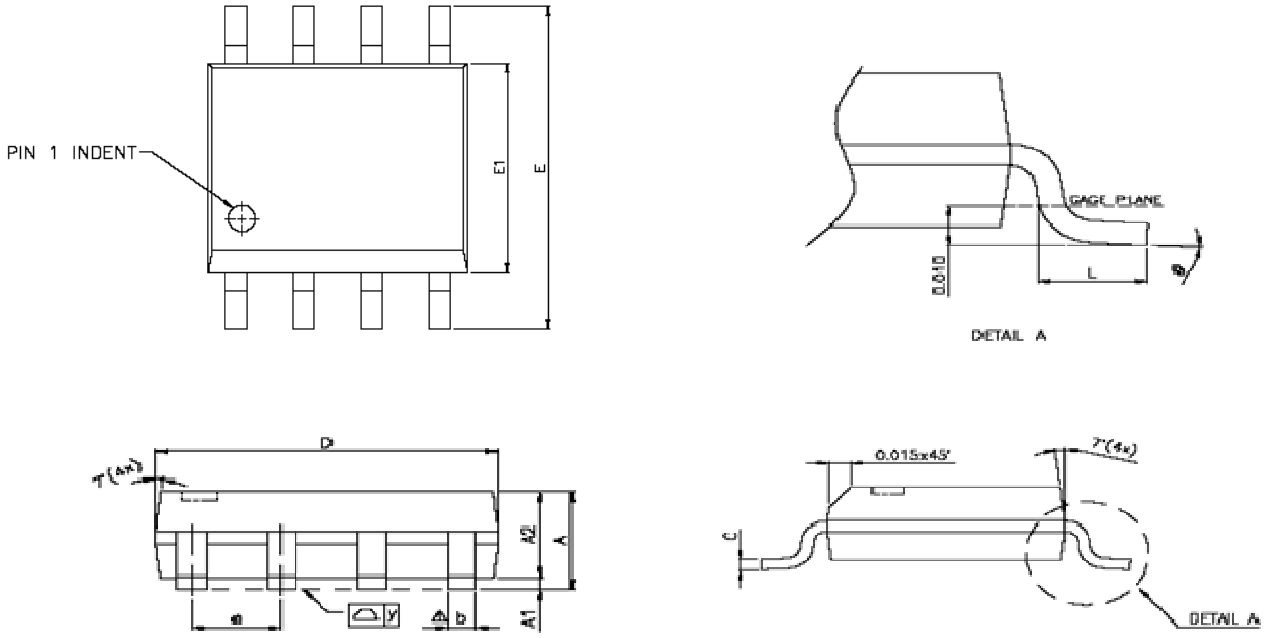


Fig. 11 Gate Charge Waveform

SOP- 8 PACKAGE OUTLINE



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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