



SPN4812

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4812 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

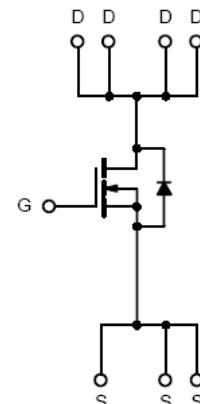
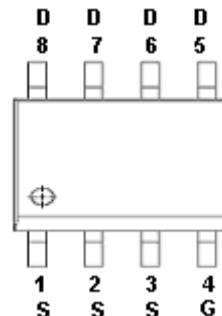
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- SMPS Secondary Side Synchronous Rectifier
- Power Tool
- Motor Control

FEATURES

- ◆ 100V/12A,R_{DS(ON)}=12mΩ@V_{GS}=10V
- ◆ 100V/12A,R_{DS(ON)}=15mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

PIN CONFIGURATION(SOP – 8P)



PART MARKING





SPN4812

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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4812S8RGB	SOP-8P	SPN4812

※ SPN4812S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	100	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	12	A
	T _A =70°C		
Pulsed Drain Current	I _{DM}	60	A
Avalanche Energy, Single Pulse (L=0.1mH , T _c =25°C)	E _{AS}	22	mJ
Power Dissipation	T _A =25°C	3.1	W
	T _A =70°C		
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient (t≤10s)	R _{θJA}	40	°C/W
Thermal Resistance-Junction to Ambient (steady state)		75	



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ELECTRICAL CHARACTERISTICS

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Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{Ds} =V _{GS} , ID=250uA	1.4	1.9	2.4	
Gate Leakage Current	I _{GSS}	V _{Ds} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{Ds} =100V, V _{GS} =0V T _J =25°C			1	uA
		V _{Ds} =100V, V _{GS} =0V T _J =100°C			100	
Drain-Source On-Resistance	R _{Ds(on)}	V _{GS} = 10V, ID=12A		9.5	12	mΩ
		V _{GS} =4.5V, ID=10A		11.5	15	
Forward Transconductance	g _f	V _{Ds} =5V, ID=12A		45		S
Diode Forward Voltage	V _{SD}	I _s =12A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge	Q _{g(10V)}	V _{Ds} =50V, V _{GS} =10V ID=14A		29		nC
Total Gate Charge	Q _{g(4.5V)}			14		
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			5		
Input Capacitance	C _{iss}	V _{Ds} =50V, V _{GS} =0V f=1MHz		2275		pF
Output Capacitance	C _{oss}			162		
Reverse Transfer Capacitance	C _{rss}			7.9		
Turn-On Time	t _{d(on)}	V _{DD} =50V, ID=14A, V _{GS} =10V R _G =10Ω		8		nS
	t _r			3		
Turn-Off Time	t _{d(off)}			26		
	t _f			4		



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

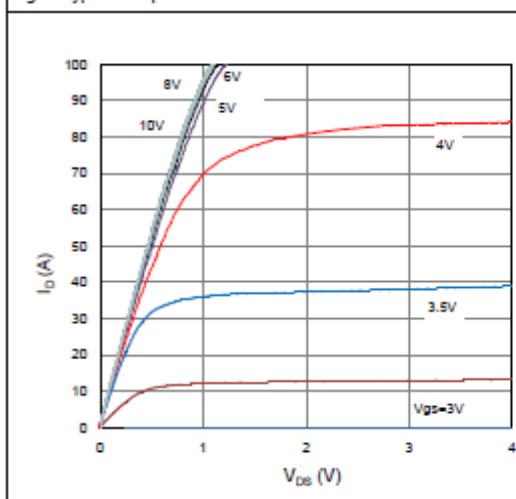


Figure 2. On-Resistance vs. Gate-Source Voltage

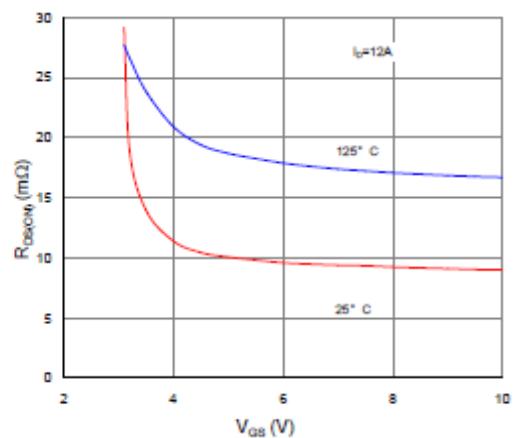


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

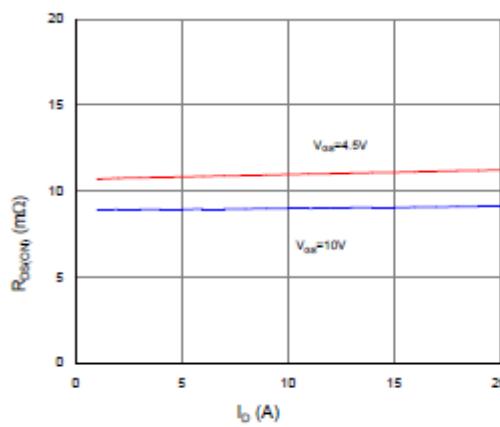


Figure 4. Normalized On-Resistance vs. Junction Temperature

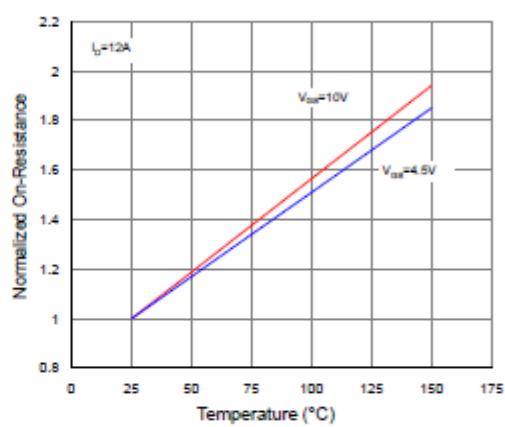


Figure 5. Typical Transfer Characteristics

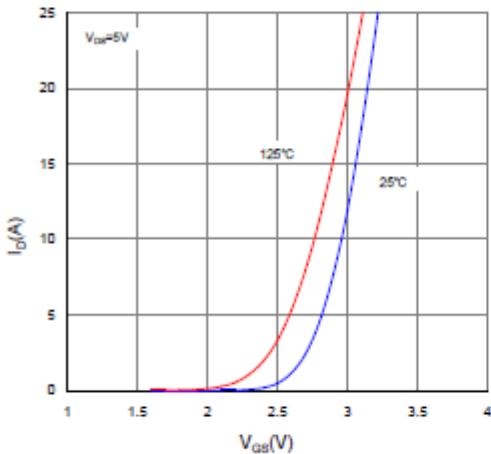
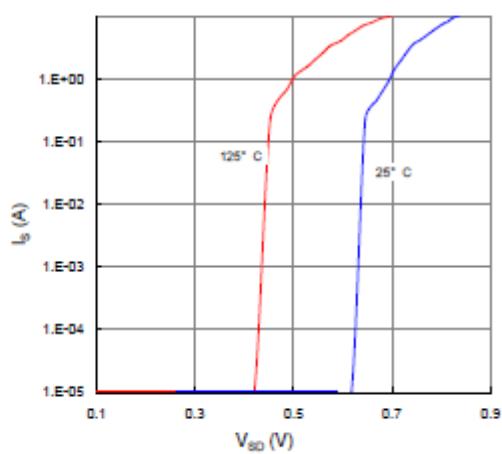


Figure 6. Typical Source-Drain Diode Forward Voltage

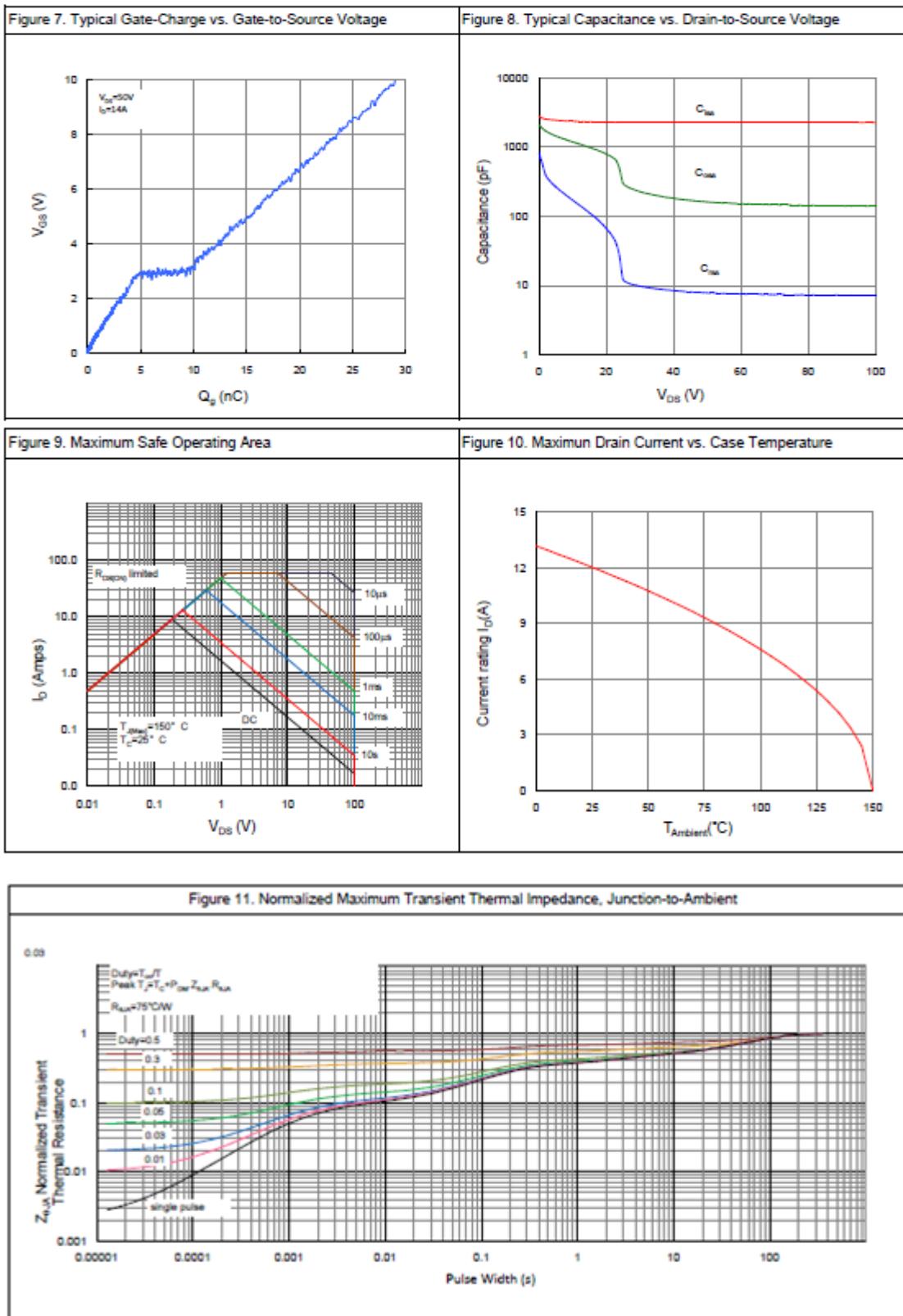




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TYPICAL CHARACTERISTICS

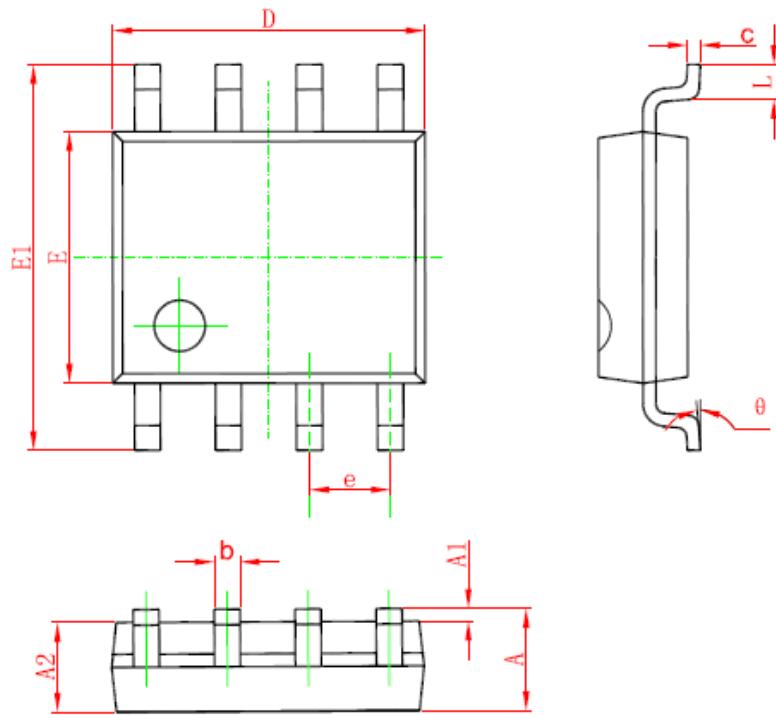




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SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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