



SPN4844

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4844 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching .

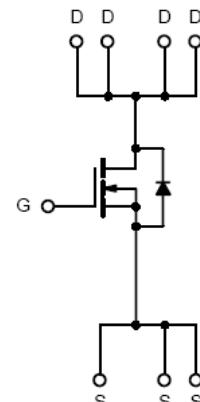
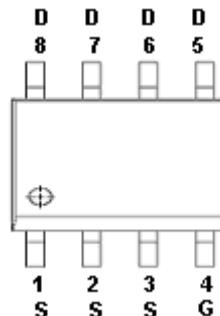
APPLICATIONS

- DC/DC Converter
- Load Switch
- Synchronous Buck Converter
- Charger Adapter
- LED Lighting

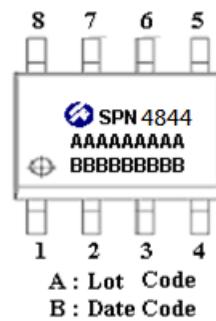
FEATURES

- ◆ 45V/15A,R_{DS(ON)}=9.5mΩ@V_{GS}=10V
- ◆ 45V/8A,R_{DS(ON)}=14mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low R_{DS (ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

PIN CONFIGURATION(SOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4844S8RGB	SOP-8P	SPN4844

※ SPN4844S8RGB : 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	45	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current	T _C =25°C	13.5	A	
	T _C =100°C	8.5		
Pulsed Drain Current	I _{DM}	50	A	
Single Pulse Avalanche Energy	E _{AS}	20	mJ	
Power Dissipation	T _C =25°C	P _D	3.1	W
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	75	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	45			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	1.0	1.55	2.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =45V, V _{GS} =0V, T _J =25 °C			1	uA
		V _{DS} =45V, V _{GS} =0V, T _J =100 °C			100	
Drain-Source On-Resistance	R _{D(on)}	V _{GS} =10V, ID=15A			9.5	mΩ
		V _{GS} =4.5V, ID=8A			14	
Forward Transconductance	g _{fs}	V _{DS} =5V, ID=10A		8		S
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q _g	V _{DS} =20V, V _{GS} =10V ID=10A		14.5		nC
Total Gate Charge (4.5V)	Q _g			7		
Gate-Source Charge	Q _{gs}			2		
Gate-Drain Charge	Q _{gd}			2.5		
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V f=1MHz		942		pF
Output Capacitance	C _{oss}			309		
Reverse Transfer Capacitance	C _{rss}			29		
Turn-On Time	t _{d(on)}	V _{DD} =20V, ID=10A, V _{GS} =10V R _G =10Ω		6		nS
	t _r			5		
Turn-Off Time	t _{d(off)}			21		
	t _f			5		
Gate resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.5		Ω



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TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

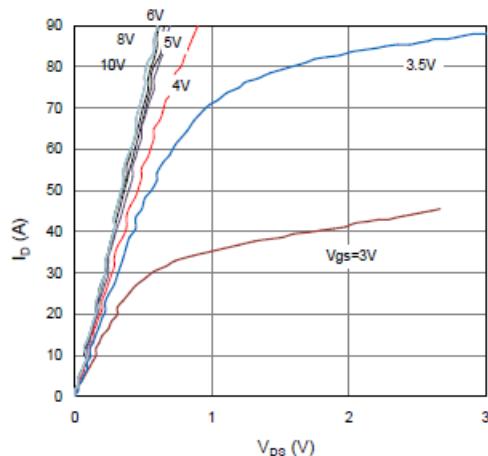


Figure 2. On-Resistance vs. Gate-Source Voltage

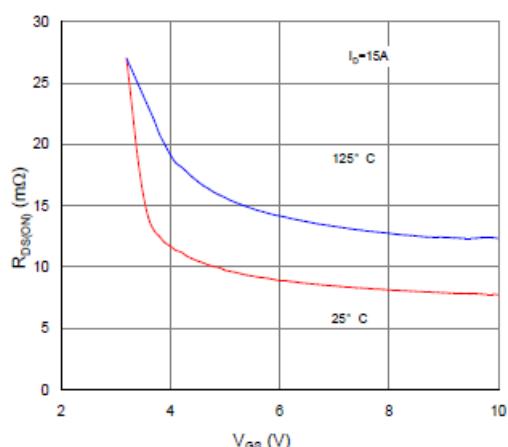


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

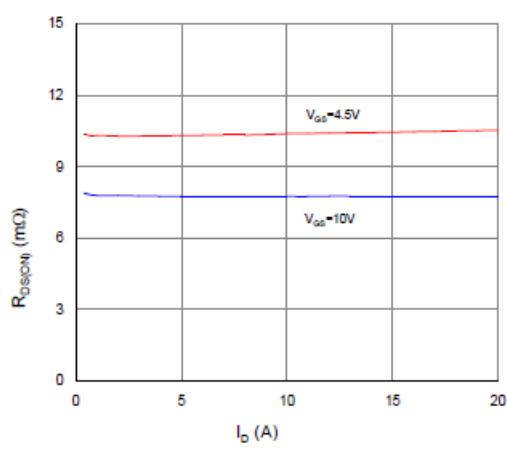


Figure 4. Normalized On-Resistance vs. Junction Temperature

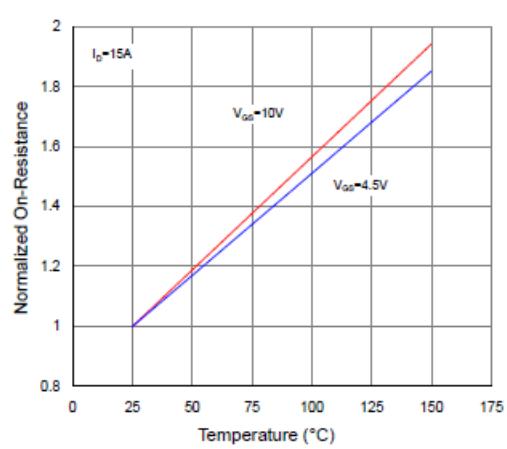


Figure 5. Typical Transfer Characteristics

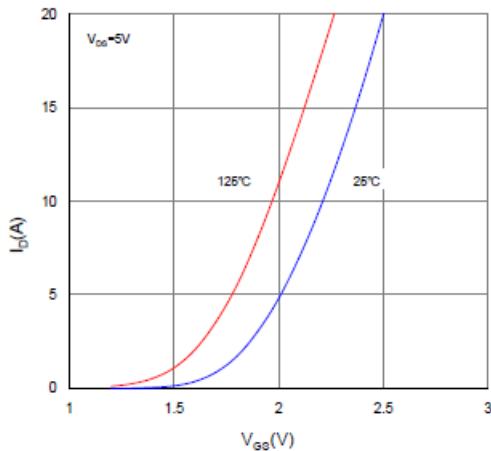
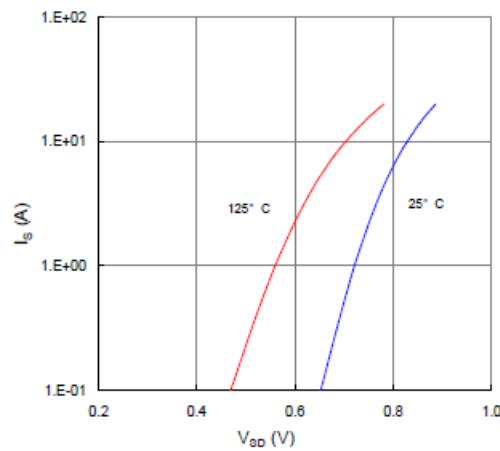


Figure 6. Typical Source-Drain Diode Forward Voltage

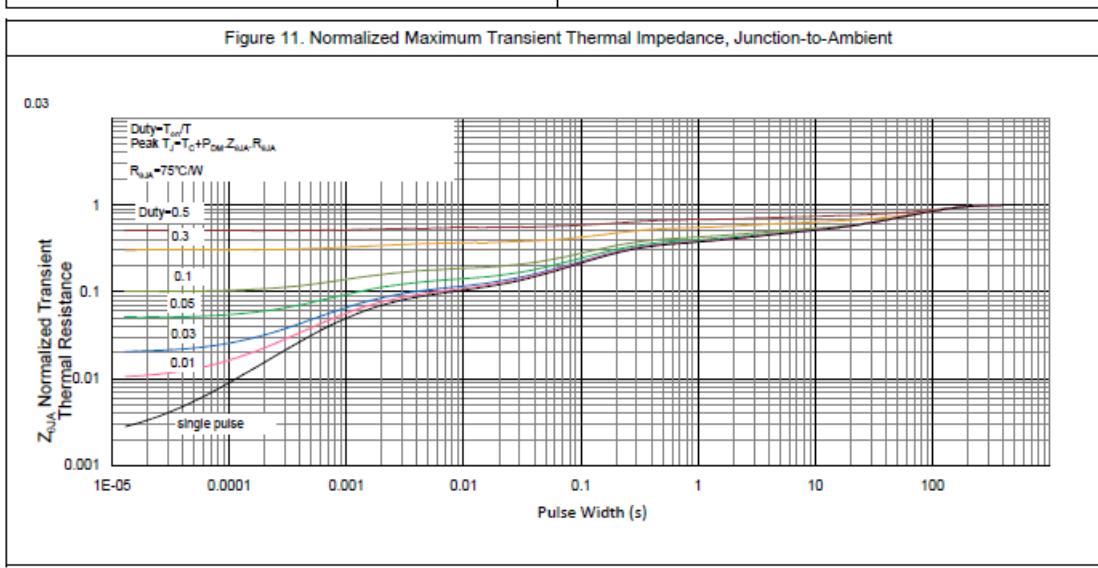
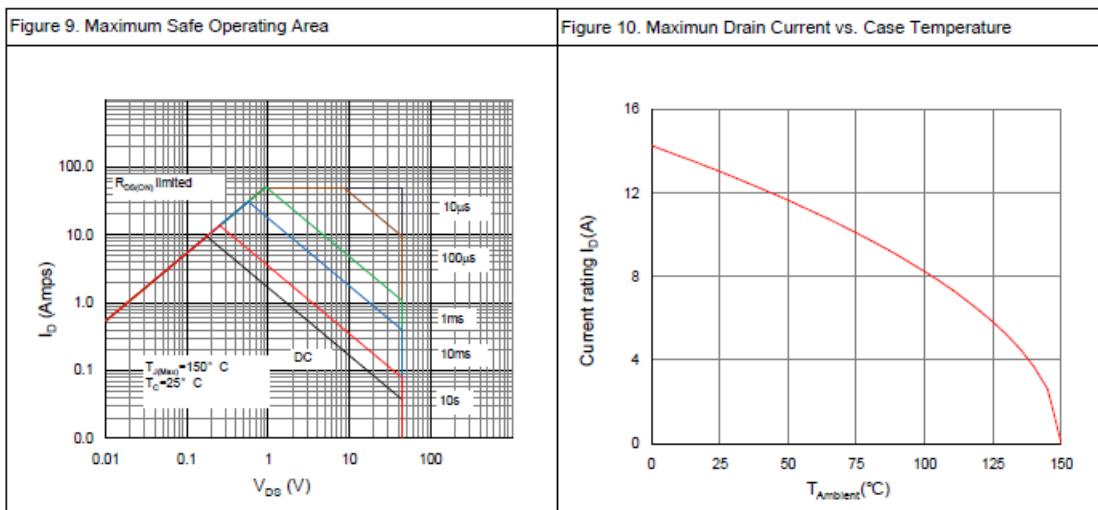
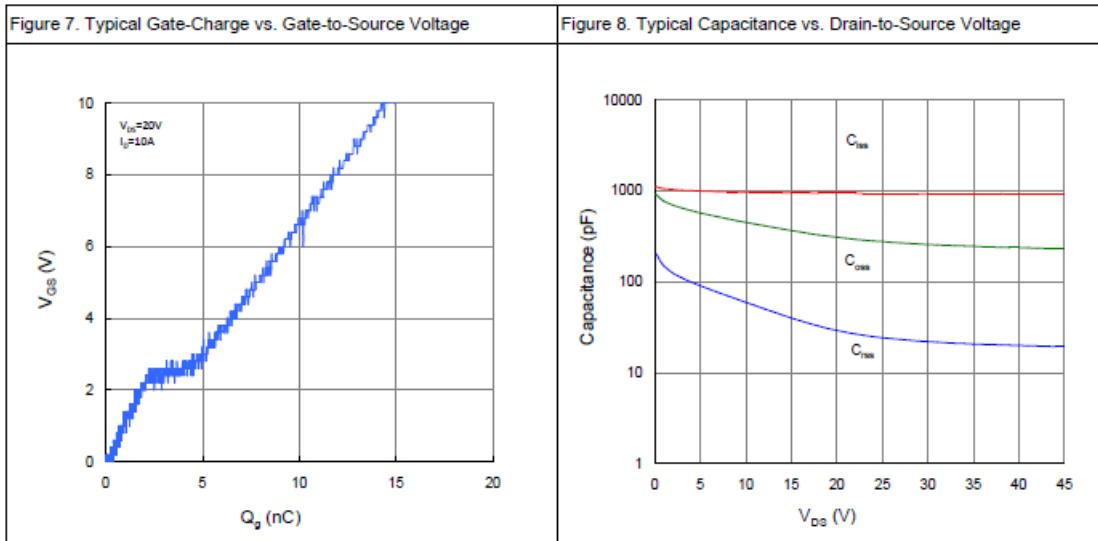




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TYPICAL CHARACTERISTICS

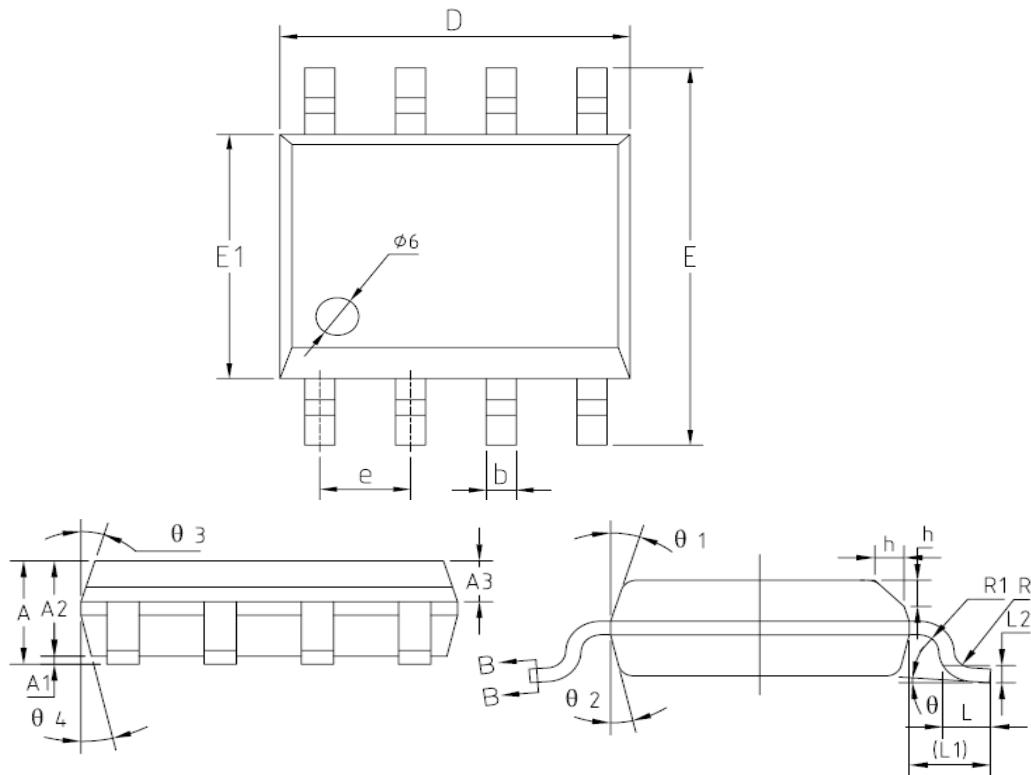




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SOP-8 PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	1.35	--	1.75
A1	0.10	--	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.33	-	0.51
c	0.17	--	0.25
D	4.80	4.93	5.05
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25BSC		
R	0.07	--	--
R1	0.07	--	0.20
h	0.25	--	0.50
θ	0°	--	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°



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