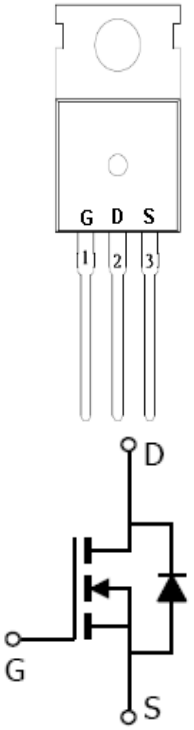
SPN50T10
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN50T10 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN80T10 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS
- Powered System
- DC/DC Converter
- Load Switch

FEATURES
- 100V/65A, $R_{DS(ON)}$=18mΩ@V_{GS}= 10V
- High density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L package design

PIN CONFIGURATION
TO-220-3L



PART MARKING


SPN50T10
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN50T10T220TGB	TO-220-3L	SPN50T10

※ SPN50T10T220TGB : Tube ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	65	A
	T_A=70℃		40	
Pulsed Drain Current		I_{DM}	200	A
Power Dissipation @ T_A=25℃		P_D	166	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0		4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V			25	uA
		V_{DS}=80V,V_{GS}=0V T_J=125℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=30A			18	mΩ
Forward Transconductance	gfs	V_{DS}=10V,I_D=30A		75		S
Diode Forward Voltage	V_{SD}	I_S=30A,V_{GS} =0V			1.3	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=80V,V_{GS}=10V I_D= 40A		115	180	nC
Gate-Source Charge	Q_{gs}			20		
Gate-Drain Charge	Q_{gd}			48		
Input Capacitance	C_{iss}	V_{DS}=25,V_{GS}=0V f=1MHz		6000	9600	pF
Output Capacitance	C_{oss}			550		
Reverse Transfer Capacitance	C_{rss}			300		
Turn-On Time	$t_{d(on)}$	V_{DD}=50V,R_L=1Ω I_D≡30A,V_{GEN}=10V R_G=1.66Ω		21		nS
	t_r			58		
Turn-Off Time	$t_{d(off)}$			41		
	t_f			15		

TYPICAL CHARACTERISTICS

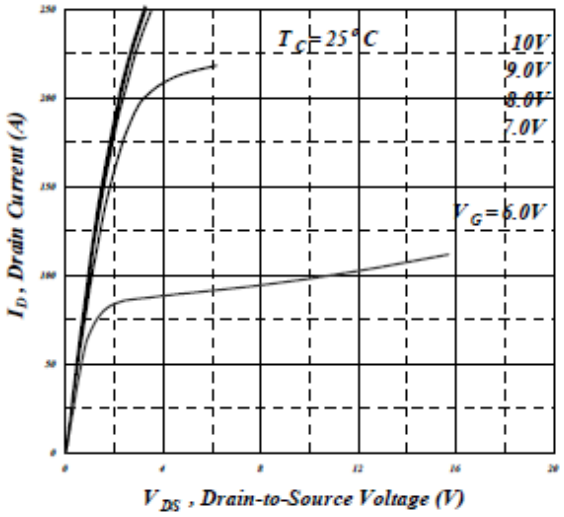


Fig 1. Typical Output Characteristics

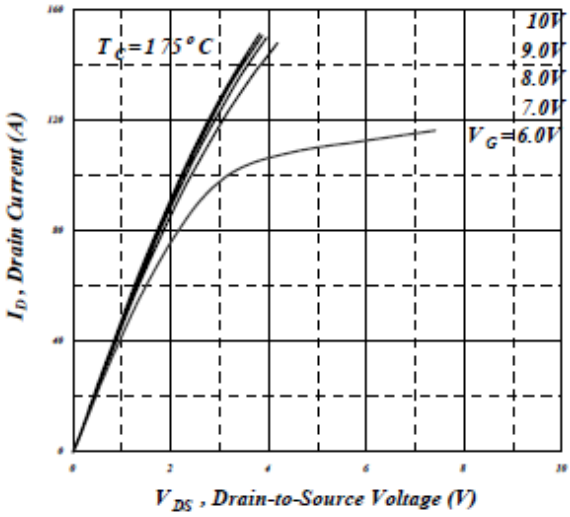


Fig 2. Typical Output Characteristics

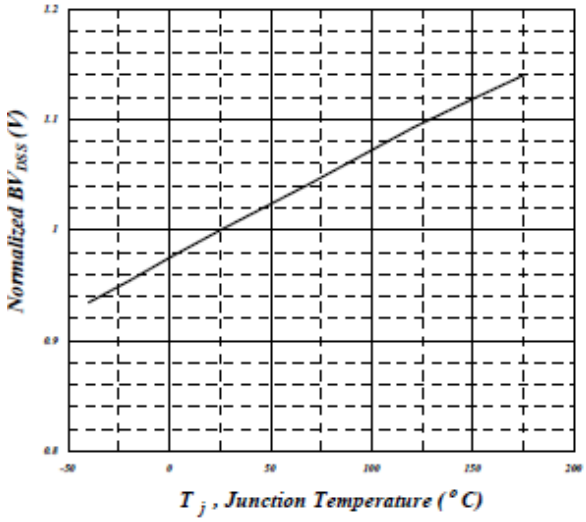


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

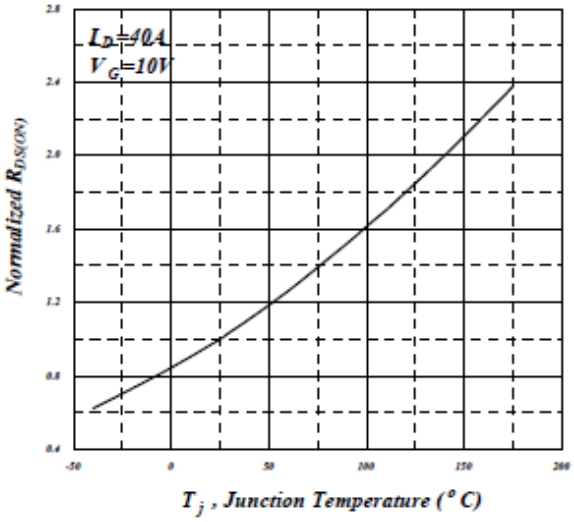


Fig 4. Normalized On-Resistance v.s. Junction Temperature

TYPICAL CHARACTERISTICS

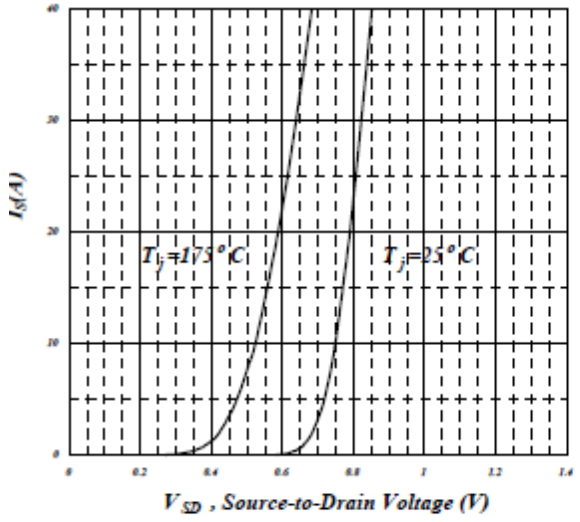


Fig 5. Forward Characteristic of Reverse Diode

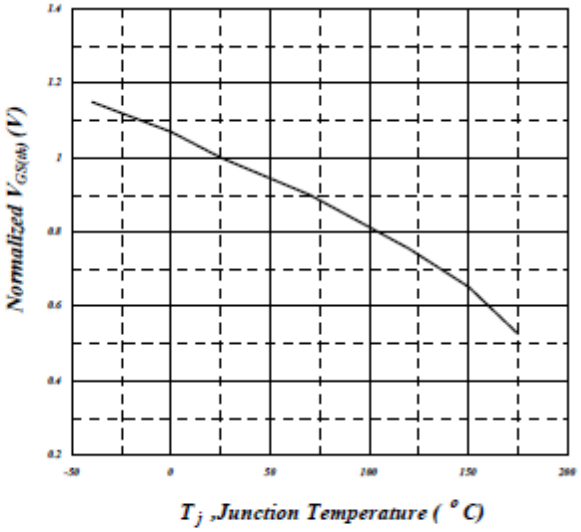


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

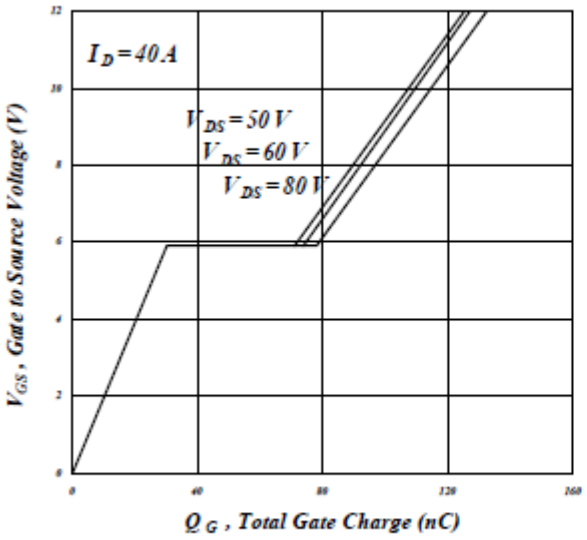


Fig 7. Gate Charge Characteristics

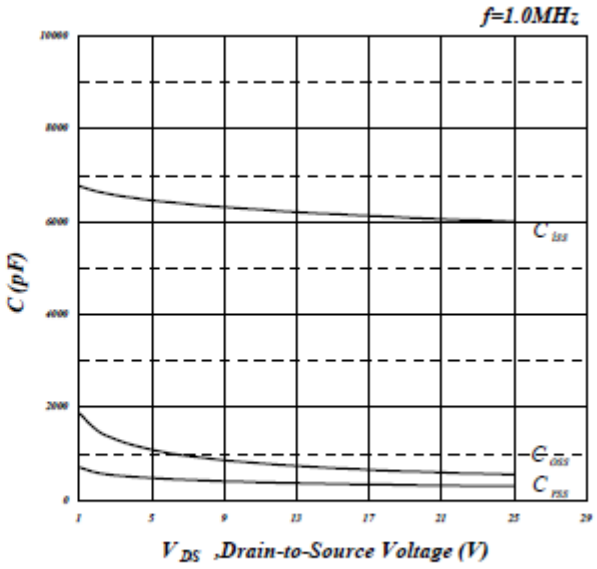


Fig 8. Typical Capacitance Characteristics

TYPICAL CHARACTERISTICS

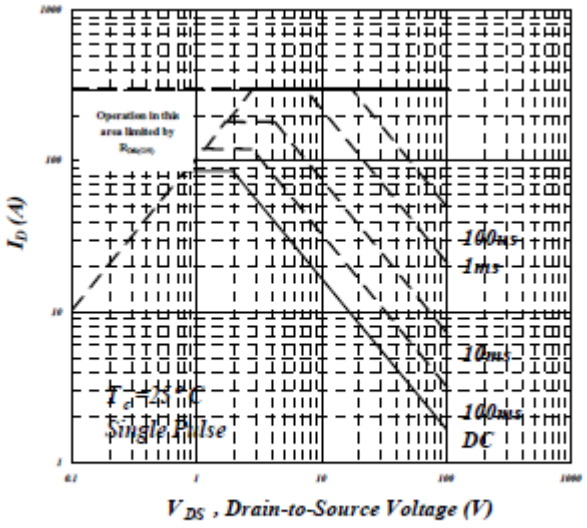


Fig 9. Maximum Safe Operating Area

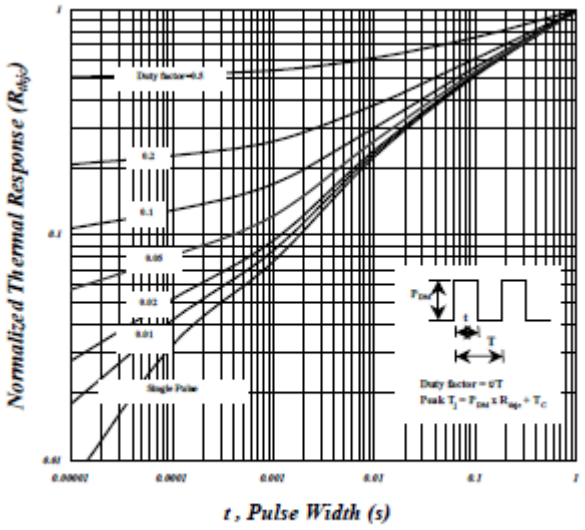


Fig 10. Effective Transient Thermal Impedance

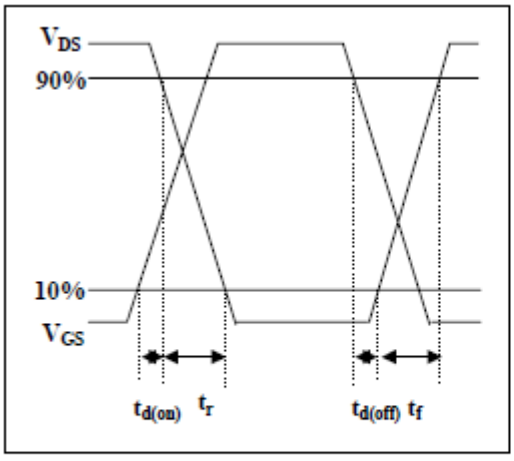


Fig 11. Switching Time Waveform

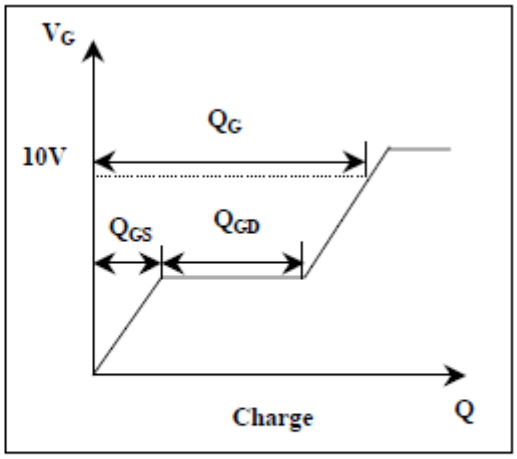
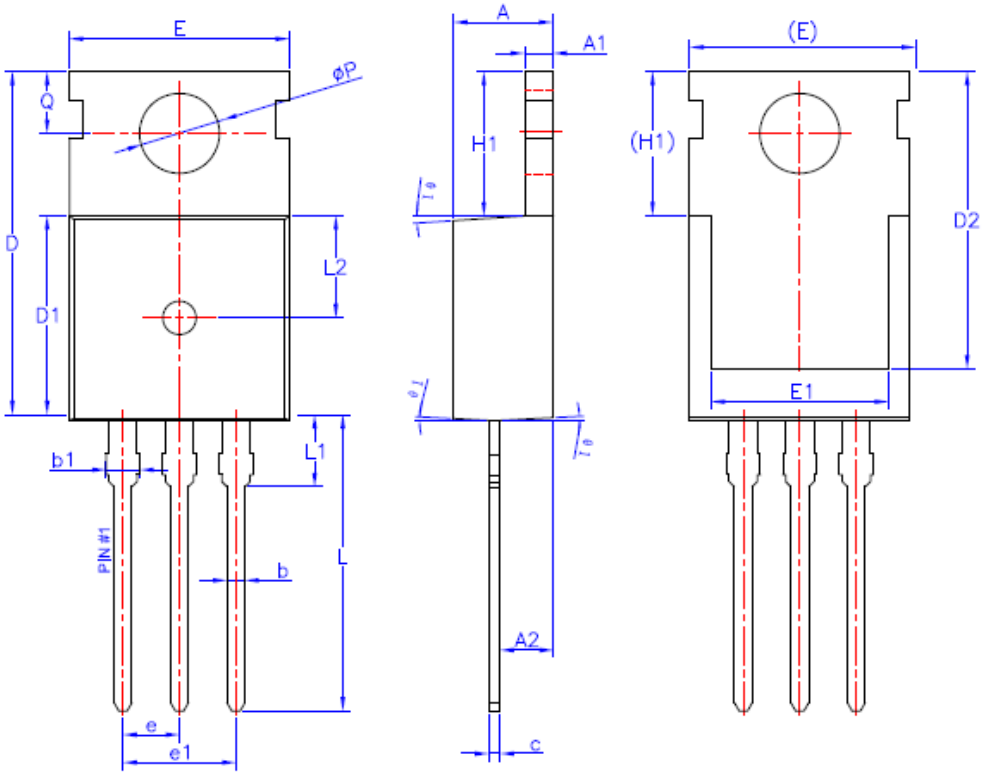


Fig 12. Gate Charge Waveform

TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	–	0.90
b1	1.42	–	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	–	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	–	–	3.50
L2	4.60REF		
ØP	3.55	3.60	3.65
Q	2.73	–	2.87
θ1	1°	3°	5°

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