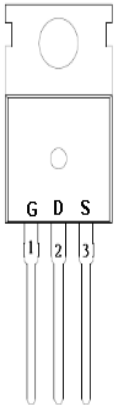
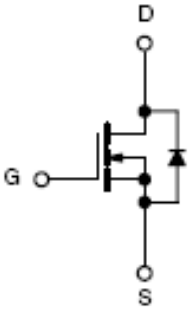
SPN6098
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN6098 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for most of synchronous buck converter applications.

APPLICATIONS
- DC/DC Converter
- Load Switch
- Synchronous Buck Converter

FEATURES
- 60V/60A, $R_{DS(ON)}$= 12mΩ@V_{GS}= 10V
- 60V/60A, $R_{DS(ON)}$= 15.0mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L package design

PIN CONFIGURATION(TO-220-3L)




PART MARKING


SPN6098
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN6098T220TG	TO-220-3L	SPN6098
SPN6098T220TGB	TO-220-3L	SPN6098

※ SPN6098T220TG: Tube ; Pb – Free
※ SPN6098T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	60	A
	T_A=100℃		47	
Pulsed Drain Current		I_{DM}	120	A
Avalanche Current		I_{AS}	38	A
Power Dissipation	T_A=25℃	P_D	62	W
Avalanche Energy with Single Pulse (Tj=25℃, L = 0.1mH , I_{AS} = 38A , V_{DD} = 25V.)		EAS	123	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V			1	uA
		V_{DS}=48V,V_{GS}=0V T_J = 55 ℃			5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≥5V,V_{GS} =10V	60			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}= 10V,I_D=15A		10	12	mΩ
		V_{GS}= 4.5V,I_D=10A		12	15	
Forward Transconductance	gfs	V_{DS}=5V,I_D=15A		47		S
Diode Forward Voltage	V_{SD}	I_S=60A,V_{GS} =0V			1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=48V,V_{GS}=4.5V I_D= 12A		24		nC
Gate-Source Charge	Q_{gs}			6.9		
Gate-Drain Charge	Q_{gd}			10		
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V f=1MHz		3200		pF
Output Capacitance	C_{oss}			210		
Reverse Transfer Capacitance	C_{rss}			145		
Turn-On Time	$t_{d(on)}$	V_{DD}=30V, I_D=2A, V_{GEN}=10V, R_G=3.3Ω		20		nS
	t_r			4		
Turn-Off Time	$t_{d(off)}$			84.5		
	t_f			6.5		

TYPICAL CHARACTERISTICS

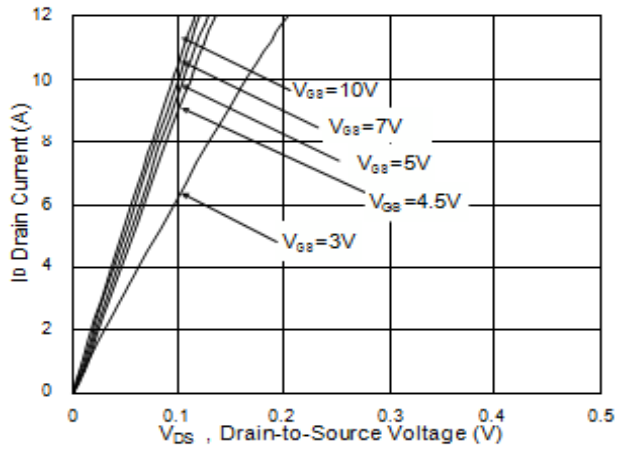


Fig. 1 Typical Output Characteristics

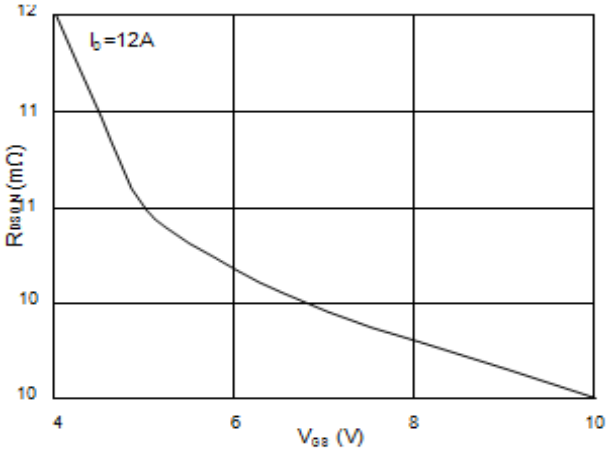


Fig. 2 On-Resistance vs. Gate Voltage

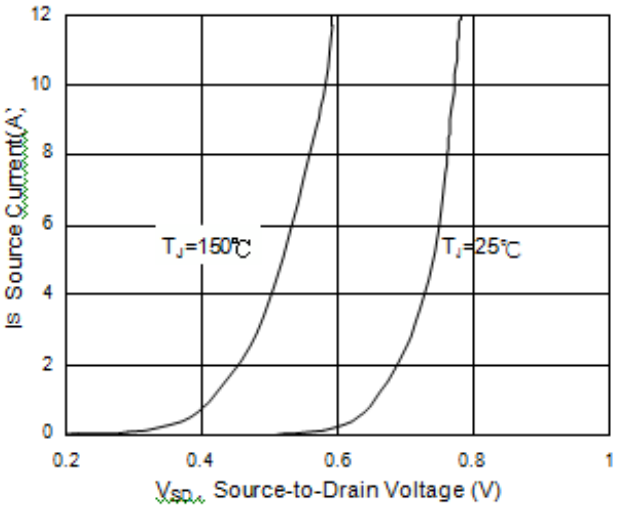


Fig. 3 Forward Characteristics Reverse Diodes

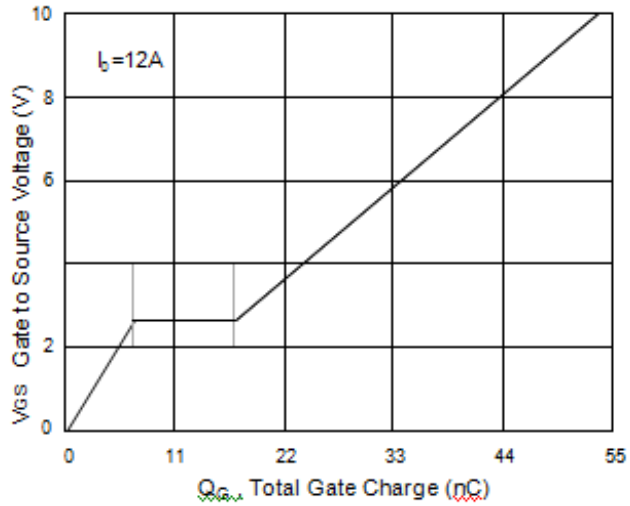


Fig. 4 Gate Charge Characteristics

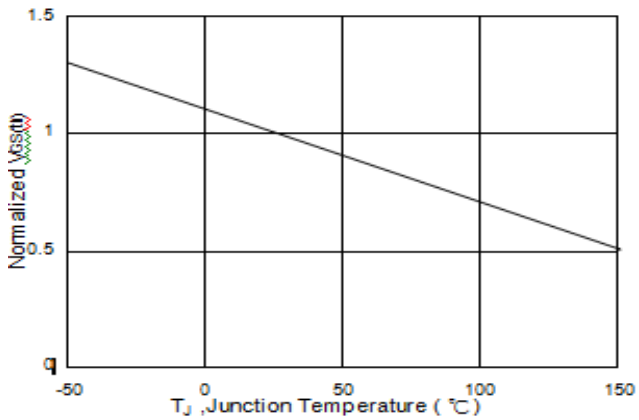


Fig. 5 Vgs vs. Junction Temperature

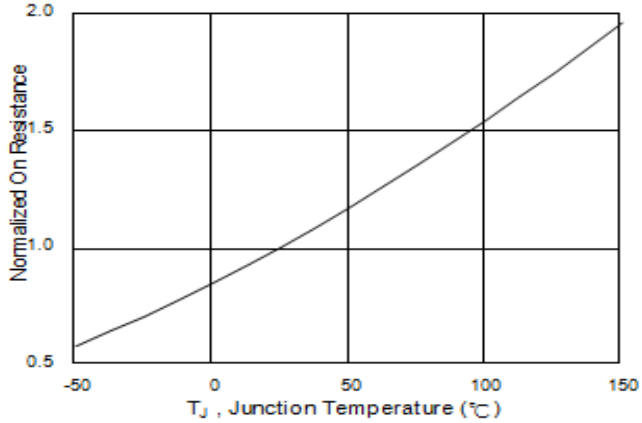


Fig. 6 On-Resistance vs. Temperature

TYPICAL CHARACTERISTICS

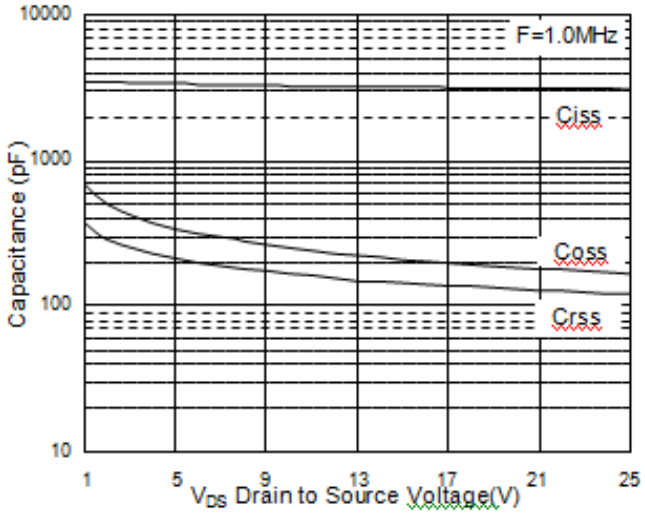


Fig. 7 Typical Capacitance Characteristics

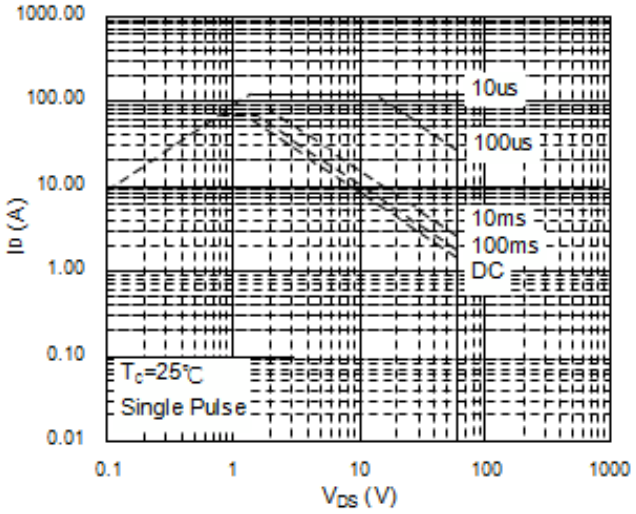


Fig. 8 Maximum Safe Operation Area

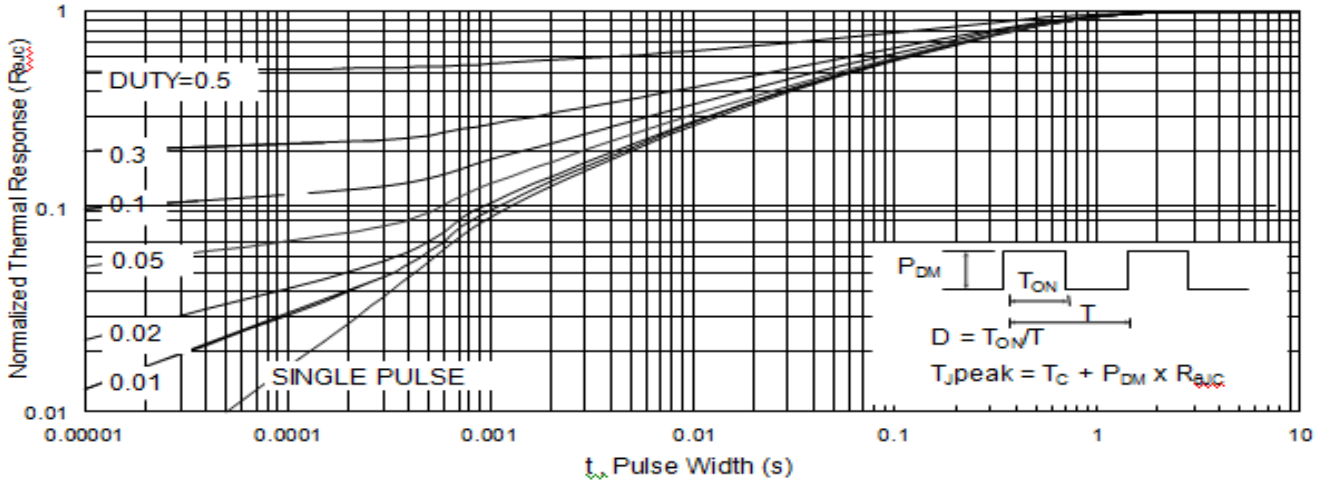


Fig. 9 Effective Transient Thermal Impedance

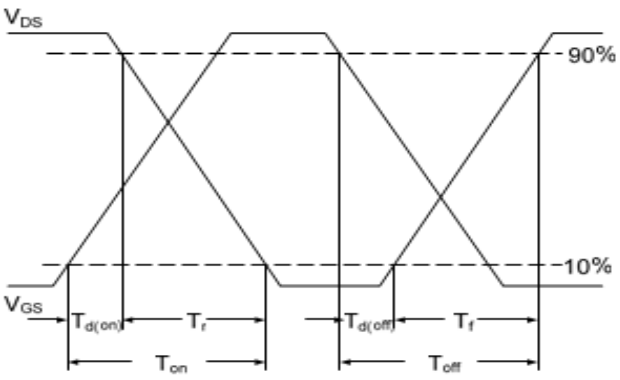


Fig. 10 Switching Time Waveform

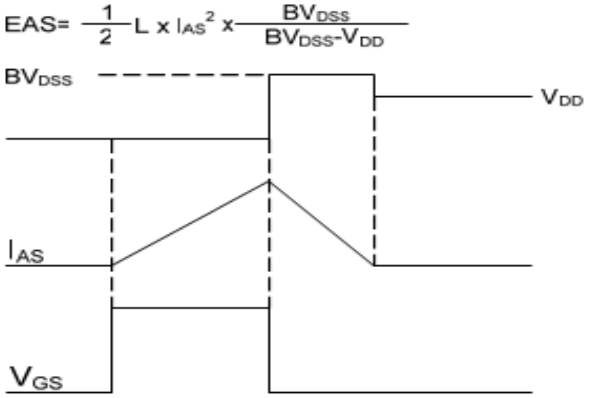
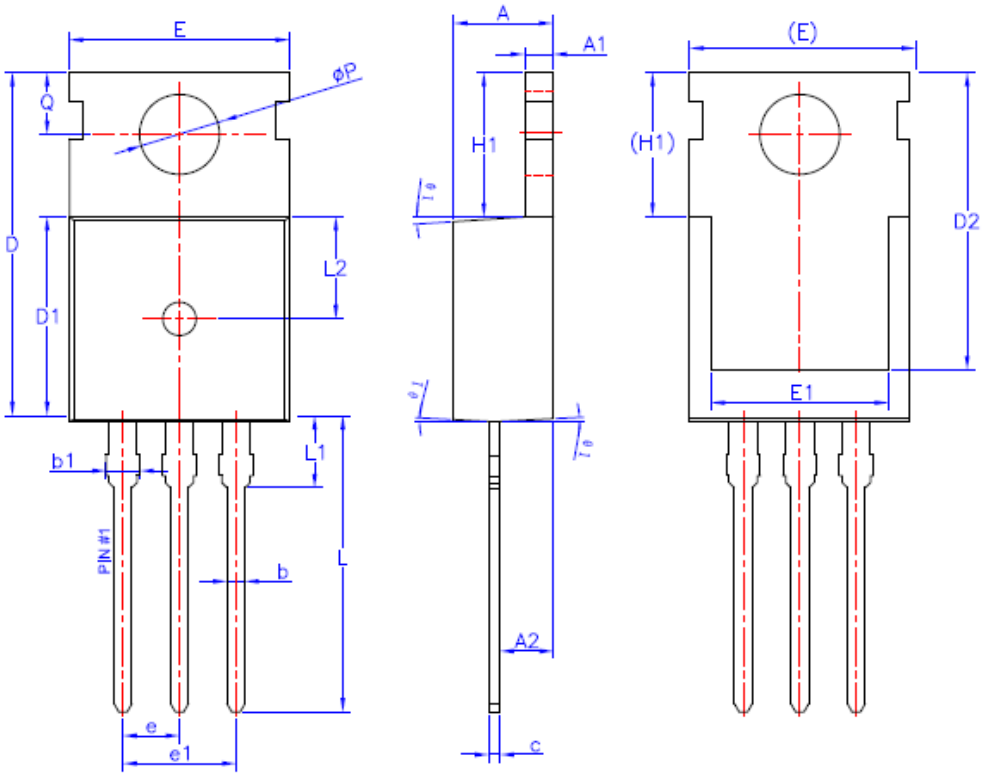


Fig. 11 Unclamped Inductive Waveform

TO-220-3L PACKAGE OUTLINE



SYMBOL	MIN	NOM	MAX
A	4.40	4.50	4.60
A1	1.27	1.30	1.33
A2	2.30	2.40	2.50
b	0.70	–	0.90
b1	1.42	–	1.57
c	0.45	0.50	0.60
D	15.30	15.70	16.10
D1	9.10	9.20	9.30
D2	13.10	–	13.70
E	9.70	9.90	10.20
E1	7.80	8.00	8.20
e	2.54BSC		
e1	5.08BSC		
H1	6.30	6.50	6.70
L	12.78	13.08	13.38
L1	–	–	3.50
L2	4.60REF		
ØP	3.55	3.60	3.65
Q	2.73	–	2.87
θ1	1°	3°	5°

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