



# SPN8205W

## Common-Drain Dual N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN8205W is the Common-Drain Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

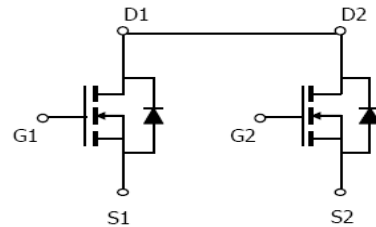
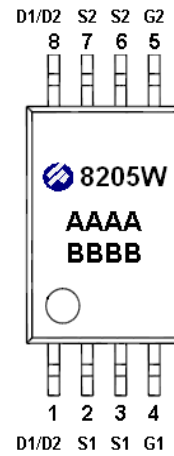
### FEATURES

- ◆ 20V/5.0A,  $R_{DS(ON)} = 24m\Omega @ V_{GS} = 4.5V$
- ◆ 20V/3.0A,  $R_{DS(ON)} = 34m\Omega @ V_{GS} = 2.5V$
- ◆ Super high density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TSSOP – 8P package design

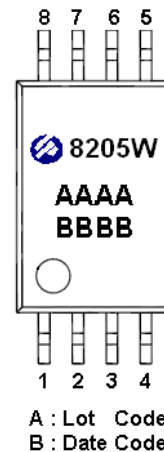
### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### PIN CONFIGURATION(TSSOP – 8P)



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	D1 / D2	Drain
2	S1	Source
3	S1	Source
4	G1	Gate
5	G2	Gate
6	S2	Source
7	S2	Source
8	D1 / D2	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8205WTS8RGB	TSSOP- 8P	8205W

※ SPN8205WTS8RG : 13" Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	20	V
Gate –Source Voltage	V <sub>GSS</sub>	±8	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	5.0
		TA=70°C	4.0
Pulsed Drain Current	I <sub>DM</sub>	20	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	2.3	A
Power Dissipation	P <sub>D</sub>	TA=25°C	1.5
		TA=70°C	0.9
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	80	°C/W



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### ELECTRICAL CHARACTERISTICS

(T<sub>A</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	-	24	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3A	-	-	34	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	0.25	-	1	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	-	18	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V	-	-	10	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = +8V, V <sub>DS</sub> =0V	-	-	+100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =5A	-	7.2	11.5	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =16V	-	0.6	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	3.4	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =10V	-	6.2	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	10	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =5V	-	15	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =10Ω	-	5	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	275	440	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =20V	-	95	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	85	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	2.2	-	Ω

### Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =0.7A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =2A, V <sub>GS</sub> =0V,	-	18.5	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	9	-	nC



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### TYPICAL CHARACTERISTICS

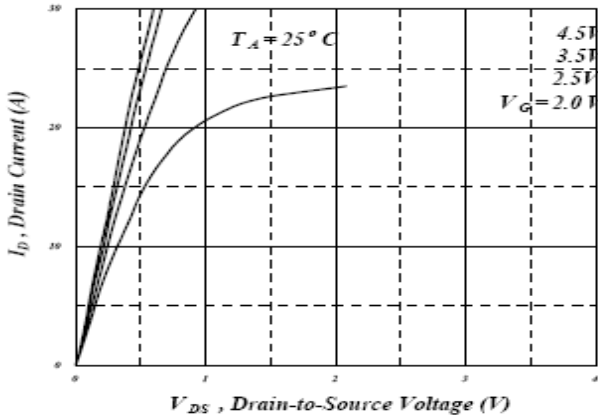


Fig 1. Typical Output Characteristics

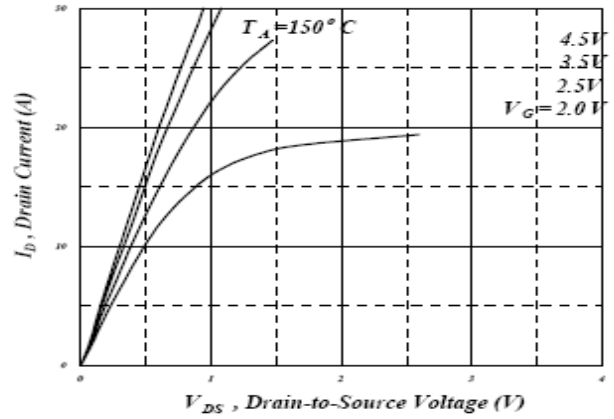


Fig 2. Typical Output Characteristics

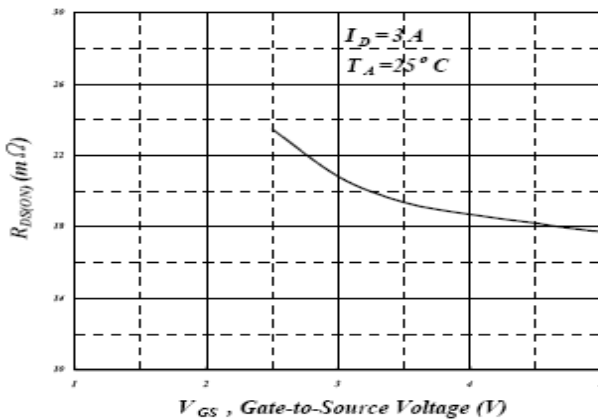


Fig 3. On-Resistance v.s. Gate Voltage

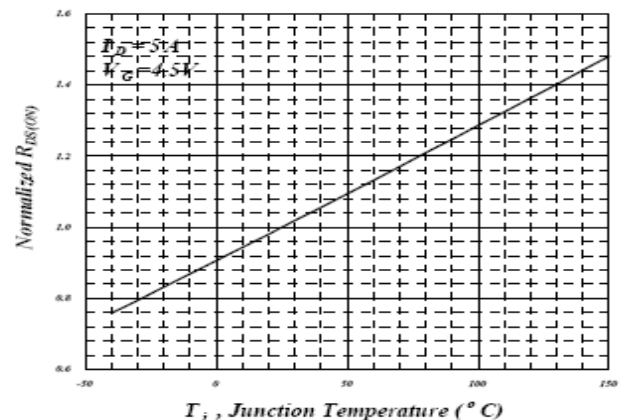


Fig 4. Normalized On-Resistance v.s. Junction Temperature

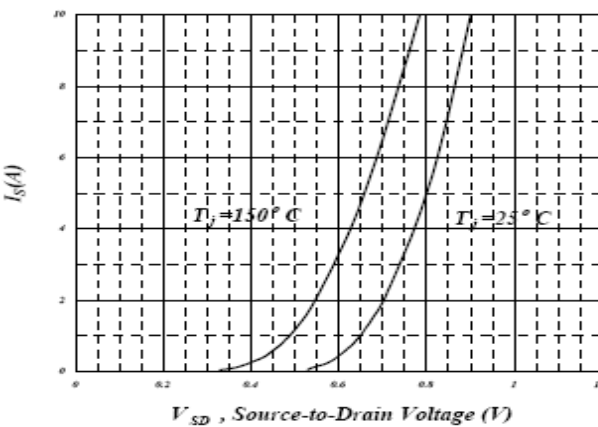


Fig 5. Forward Characteristic of Reverse Diode

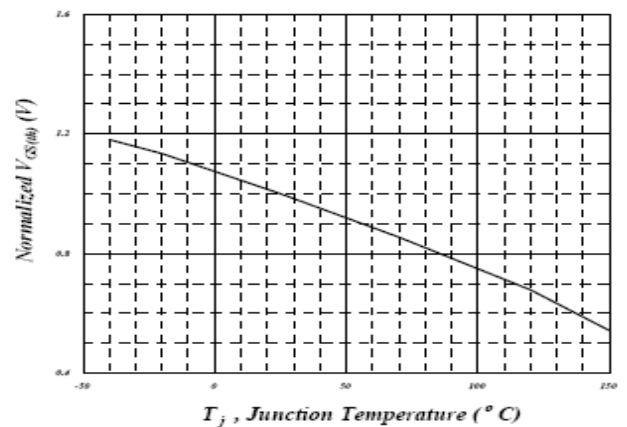


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



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### TYPICAL CHARACTERISTICS

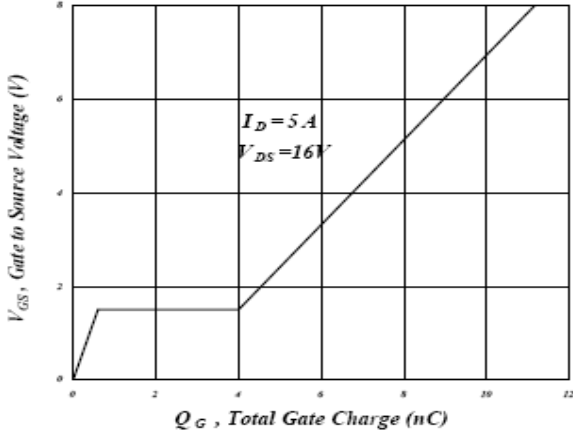


Fig 7. Gate Charge Characteristics

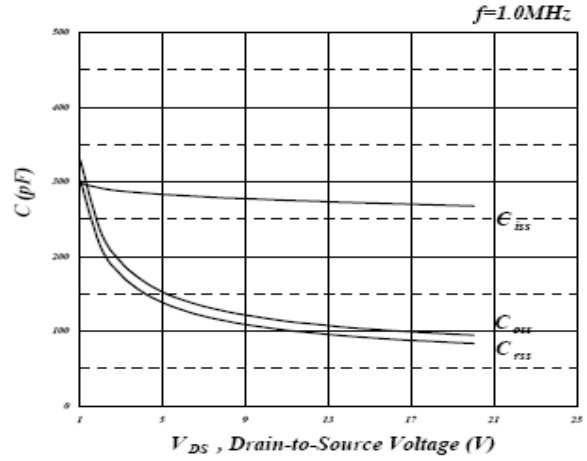


Fig 8. Typical Capacitance Characteristics

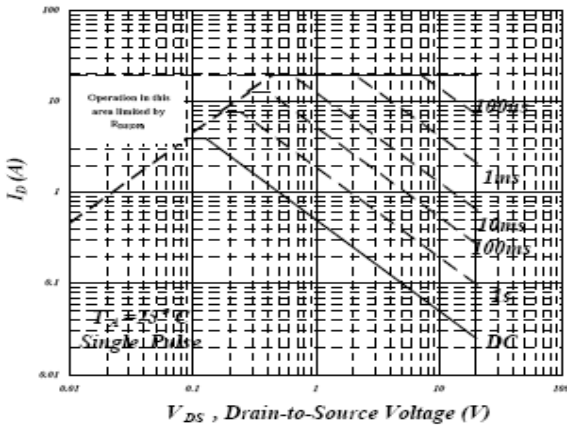


Fig 9. Maximum Safe Operating Area

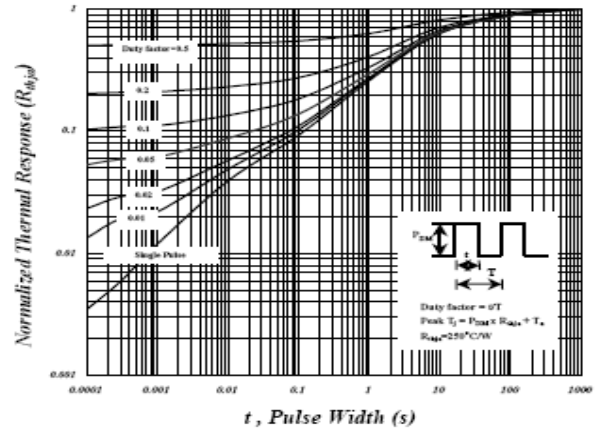


Fig 10. Effective Transient Thermal Impedance

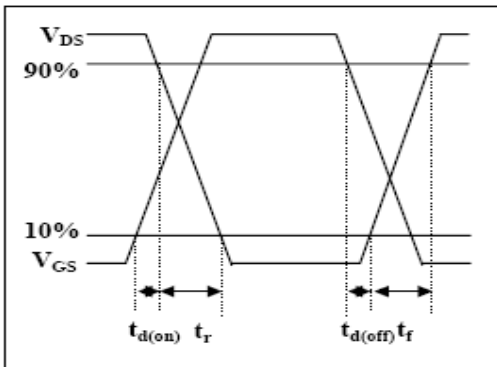


Fig 11. Switching Time Waveform

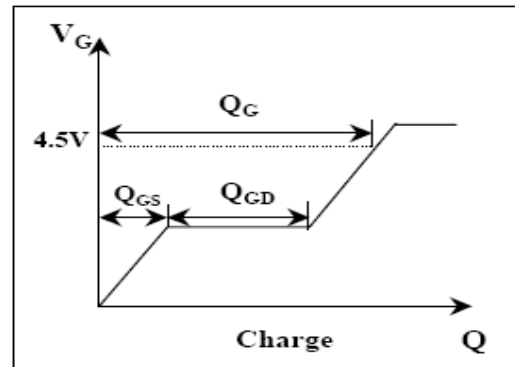


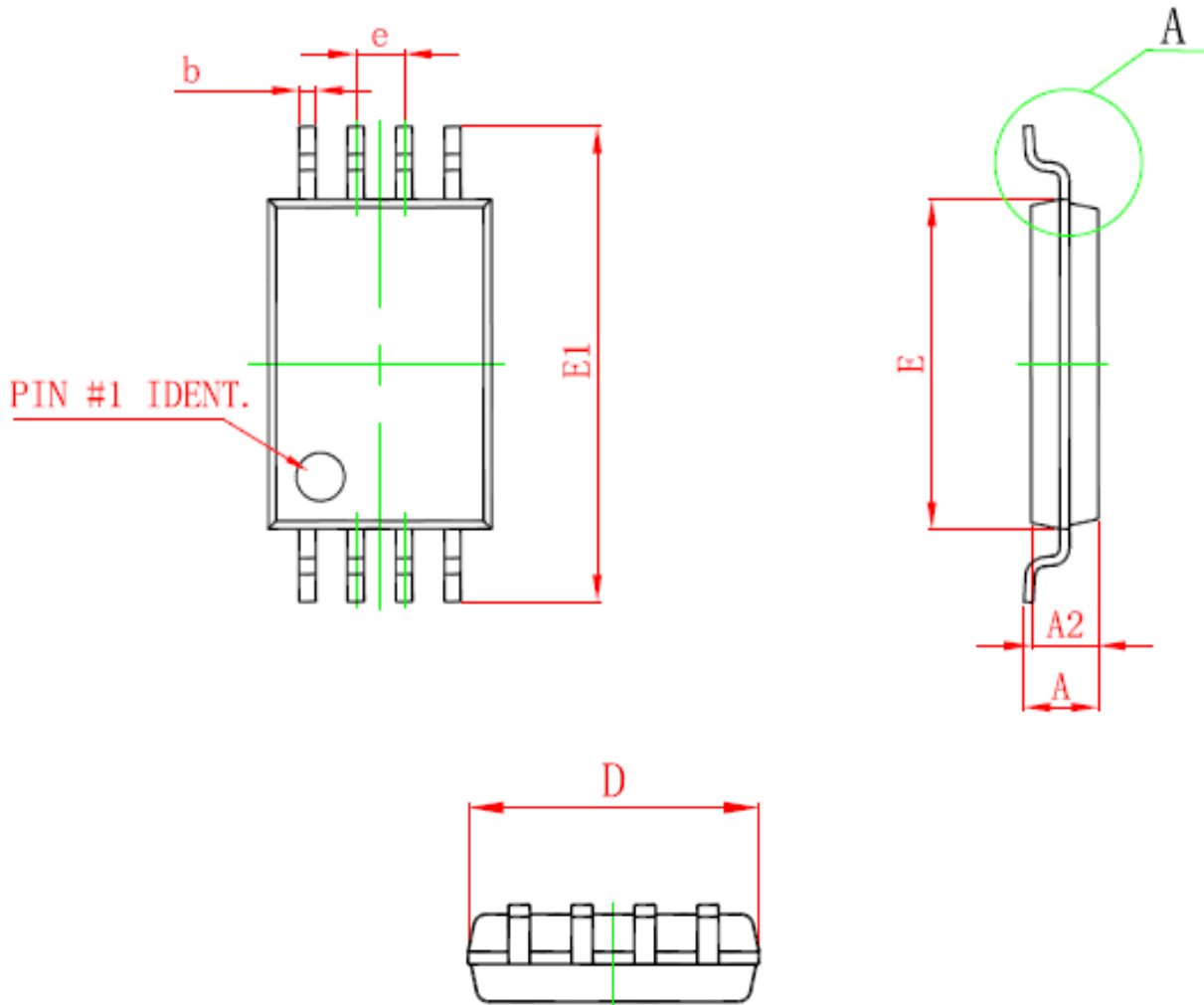
Fig 12. Gate Charge Waveform



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## TSSOP- 8P PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°



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