



SPN8439 N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8439 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

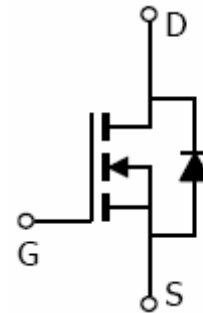
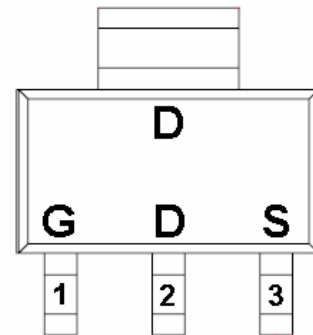
FEATURES

- ◆ 30V/6.2A, $R_{DS(ON)} = 42m\Omega @ V_{GS} = 4.5V$
- ◆ 30V/5.4A, $R_{DS(ON)} = 54m\Omega @ V_{GS} = 2.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-223 package design

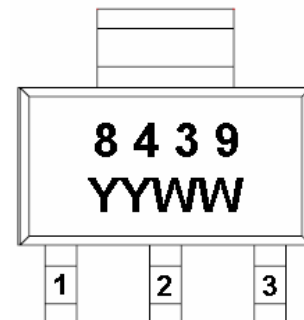
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION(SOT-223)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8439S223RG	SOT-223	8439

※ SPN8439S223RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V_{DSS}	30	V	
Gate –Source Voltage	V_{GSS}	± 12	V	
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	5.8	A
		$T_A=70^{\circ}\text{C}$	4.2	
Pulsed Drain Current	I_{DM}	25	A	
Continuous Source Current(Diode Conduction)	I_S	1.7	A	
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	2.8	W
		$T_A=70^{\circ}\text{C}$	1.2	
Operating Junction Temperature	T_J	150	$^{\circ}\text{C}$	
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	90	$^{\circ}\text{C}/\text{W}$	



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ELECTRICAL CHARACTERISTICS

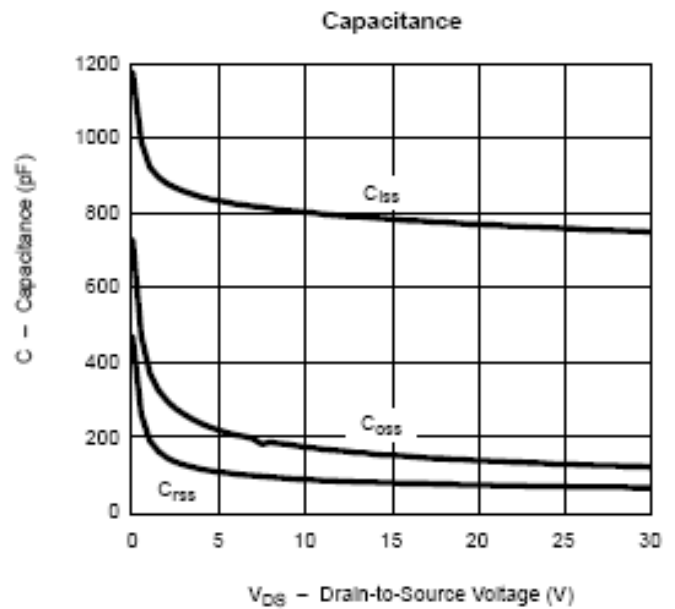
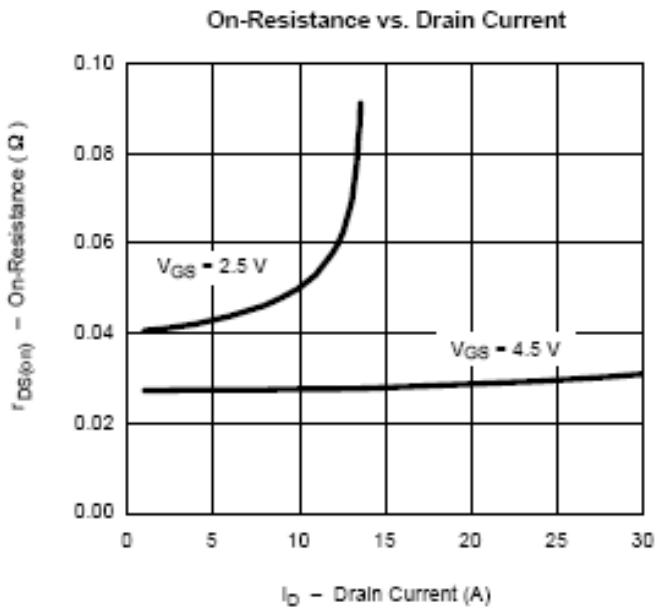
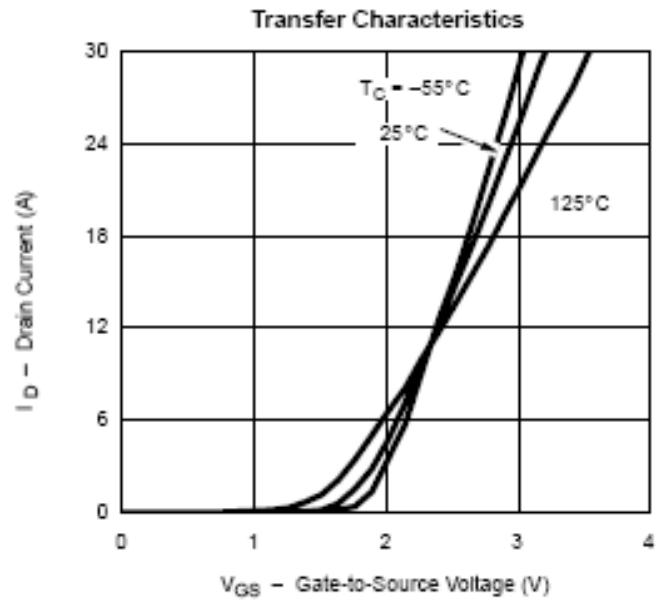
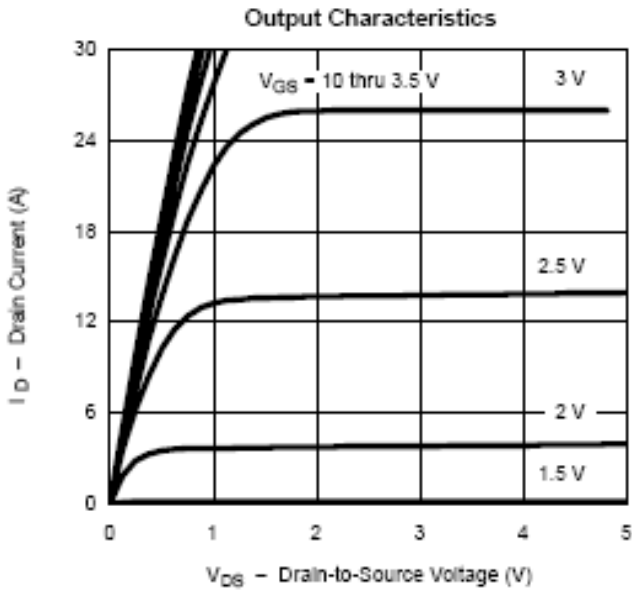
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	0.8		1.6	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V, V _{GS} =1.0V			1	uA
		V _{DS} =24V, V _{GS} =0.0V T _J =55°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥ 4.5V, V _{GS} =4.5V	10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =6.2A		0.034	0.042	Ω
		V _{GS} =2.5V, I _D =5.4A		0.040	0.054	
Forward Transconductance	g _{fs}	V _{DS} =4.5V, I _D =5.4A		12		S
Diode Forward Voltage	V _{SD}	I _S =1.7A, V _{GS} =0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =10V I _D =6.7A		10	18	nC
Gate-Source Charge	Q _{gs}			1.6		
Gate-Drain Charge	Q _{gd}			3.2		
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz		450		pF
Output Capacitance	C _{oss}			240		
Reverse Transfer Capacitance	C _{rss}			38		
Turn-On Time	t _{d(on)}	V _{DD} =15V, R _L =15 I _D =1.0A, V _{GEN} =10 R _G =6Ω		7	15	ns
	t _r			10	20	
Turn-Off Time	t _{d(off)}			20	40	
	t _f			11	20	



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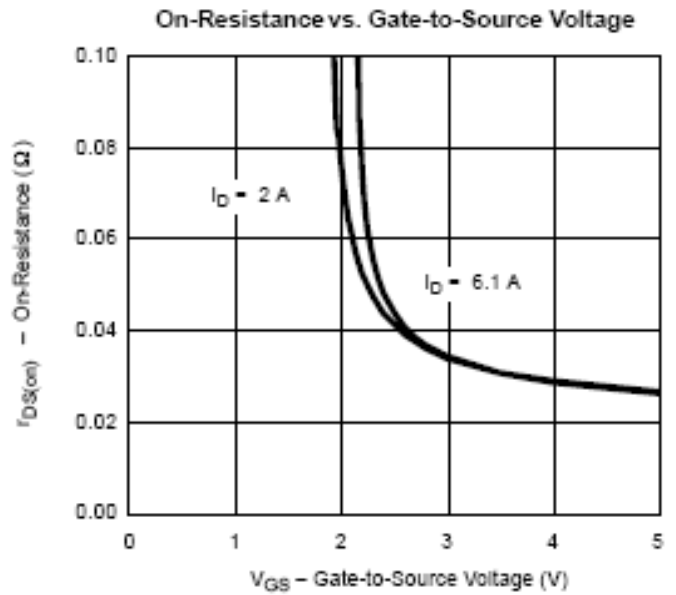
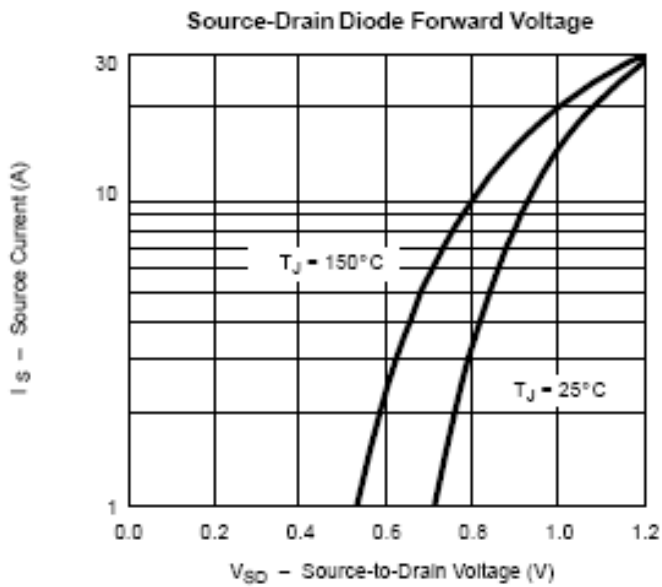
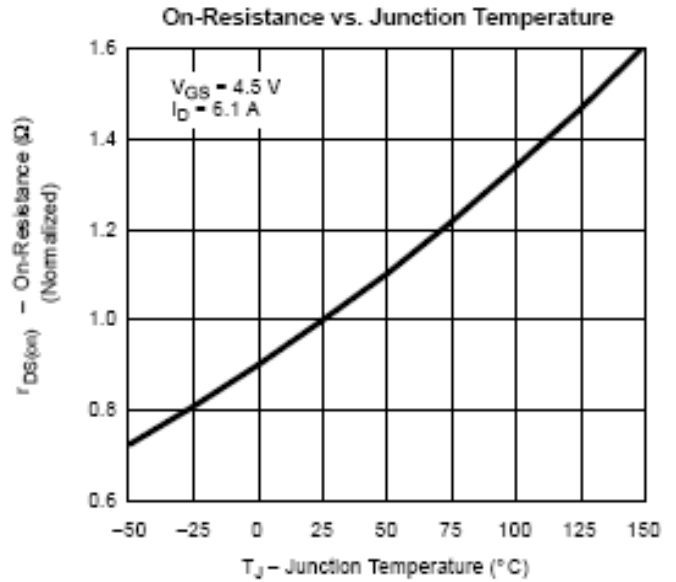
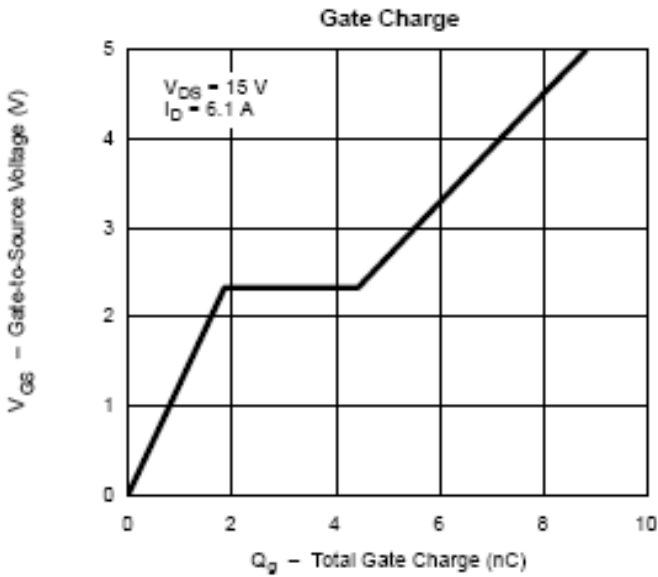
TYPICAL CHARACTERISTICS





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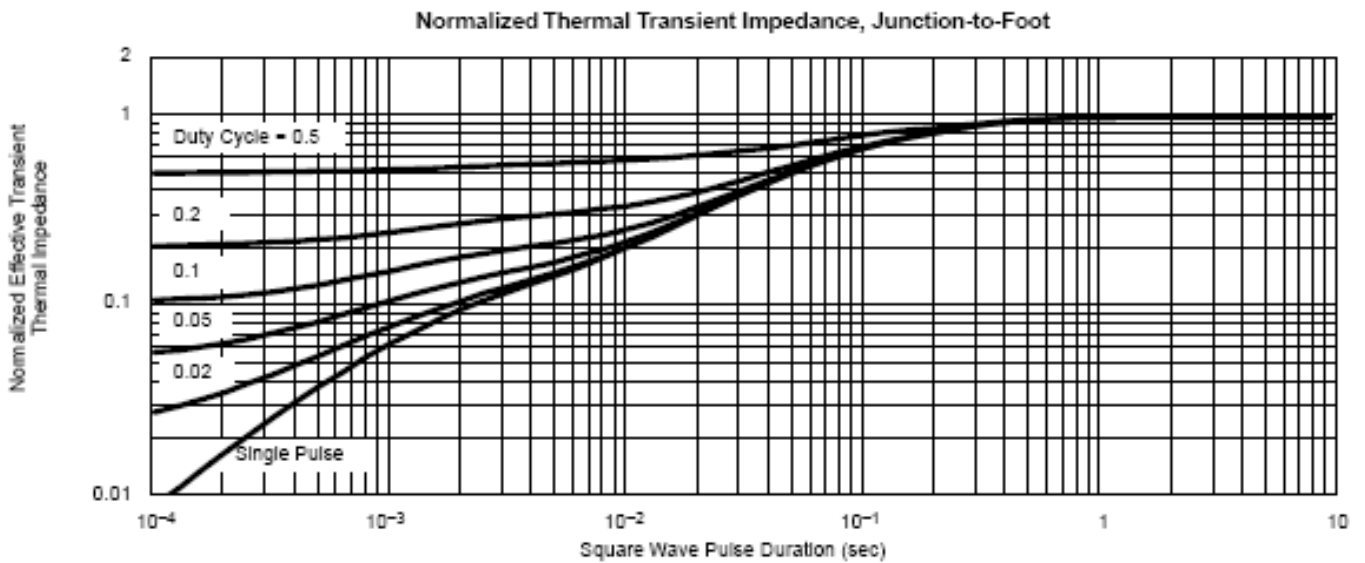
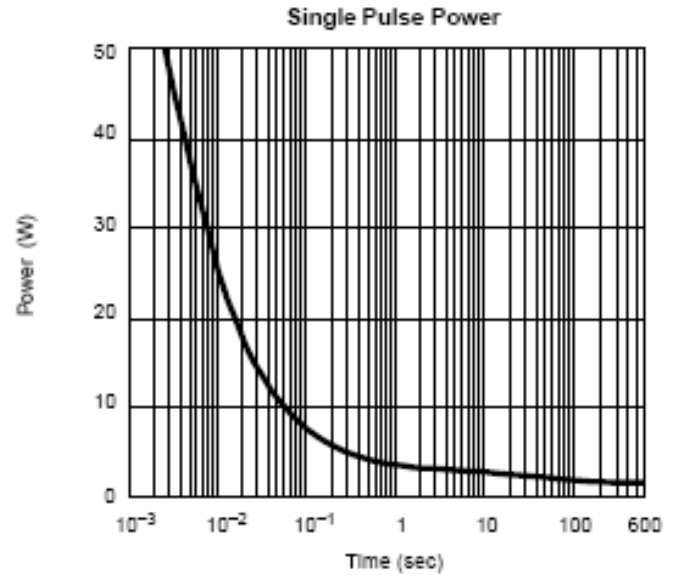
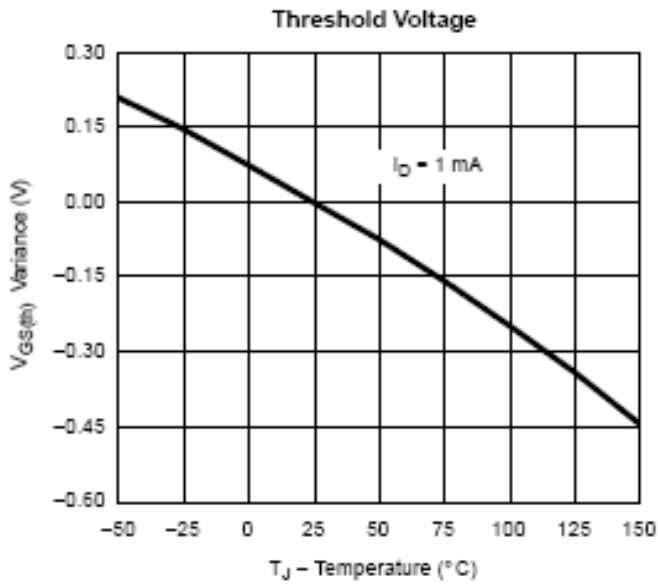
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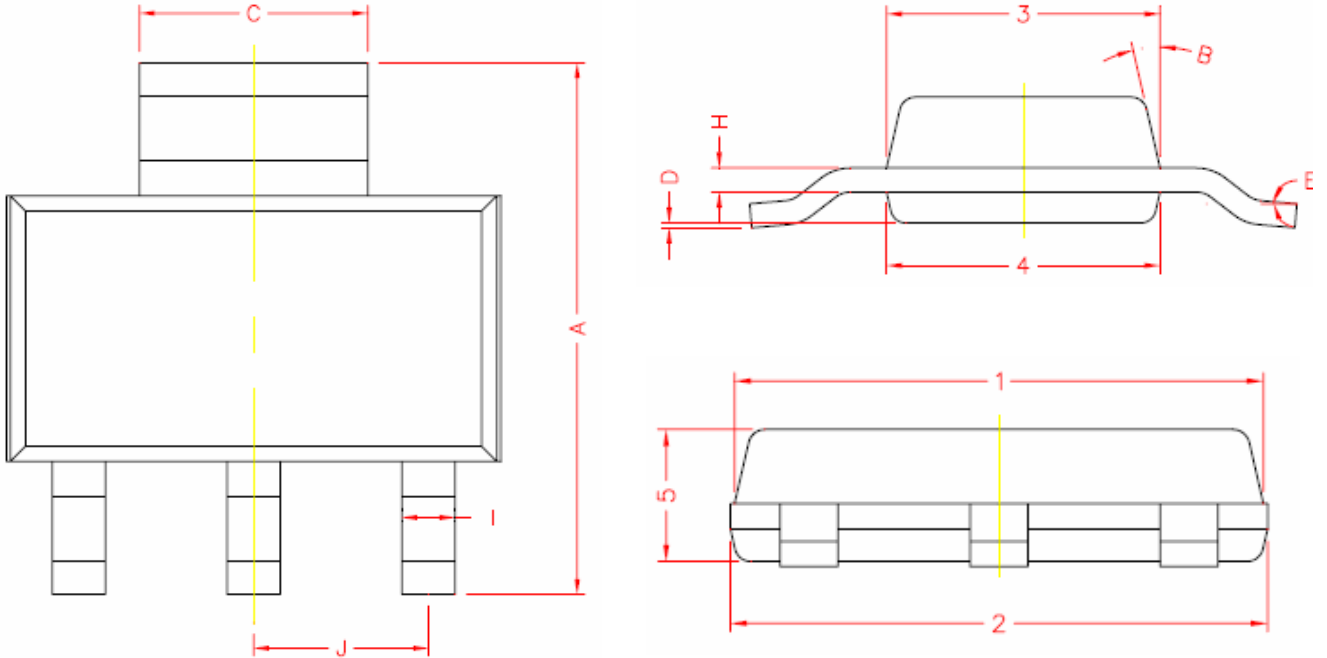




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SOT-233 PACKAGE OUTLINE



REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	6.70	7.30
C	2.90	3.10
D	0.02	0.10
E	0°	10°
I	0.60	0.80
H	0.25	0.35
B	13° TYP.	
J	2.30 REF.	
1	6.30	6.70
2	6.30	6.70
3	3.30	3.70
4	3.30	3.70
5	1.40	1.80



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