



SPN8457

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8457 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

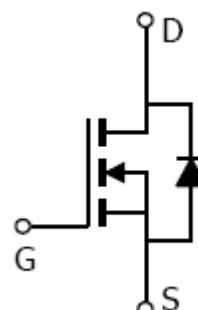
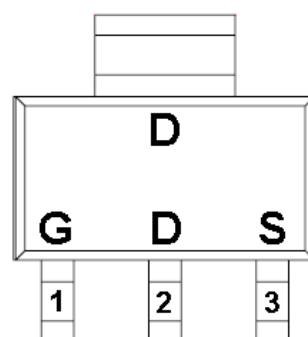
FEATURES

- ◆ 30V/5.5A,R_{DS(ON)}=58mΩ@V_{GS}=10V
- ◆ 30V/4.0A,R_{DS(ON)}=98mΩ@V_{GS}=4.5V
- ◆ Super high density cell design for extremely low R_{DS (ON)}
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-223 package design

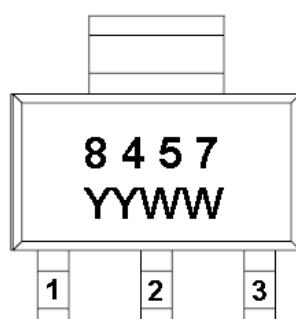
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION(SOT-223)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8457S22RG	SOT-223	8457

※ SPN8457S22RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate –Source Voltage	V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	ID	5.8
	T _A =70°C		4.2
Pulsed Drain Current	I _{DM}	10	A
Continuous Source Current(Diode Conduction)	I _S	1.25	A
Power Dissipation	T _A =25°C	P _D	2.8
	T _A =70°C		1.2
Operating Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W



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ELECTRICAL CHARACTERISTICS

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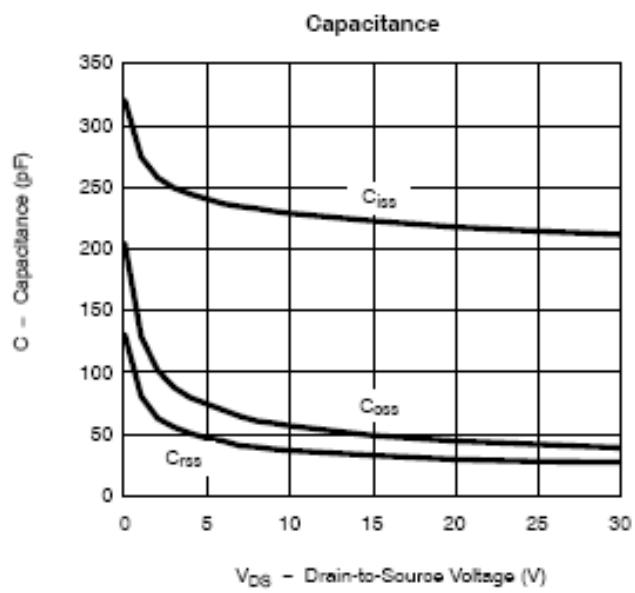
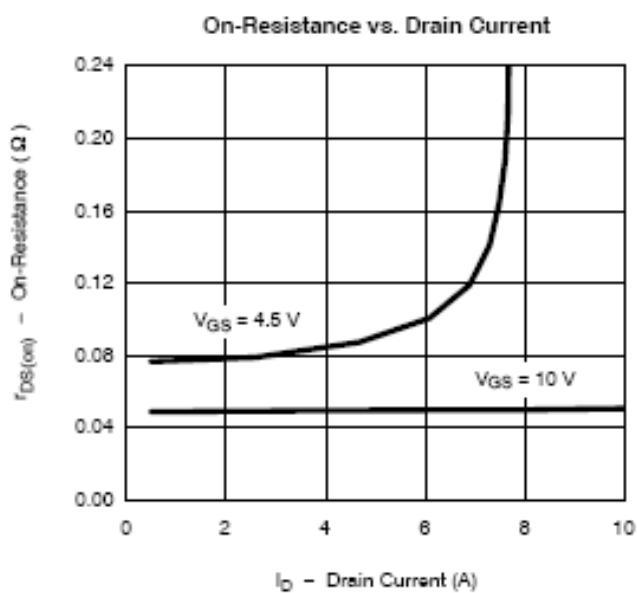
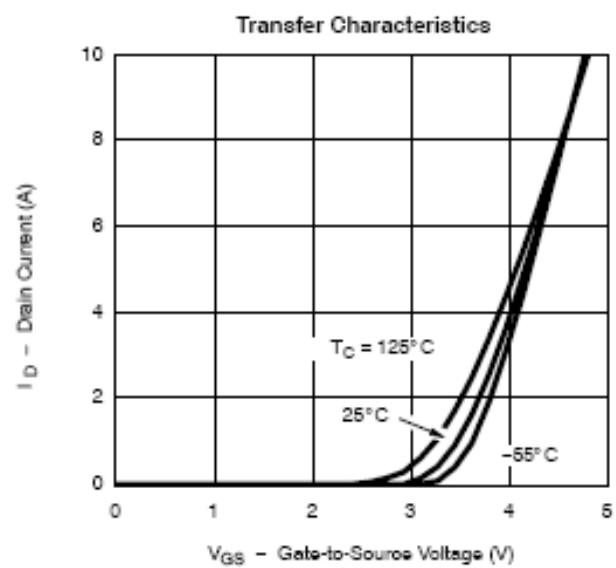
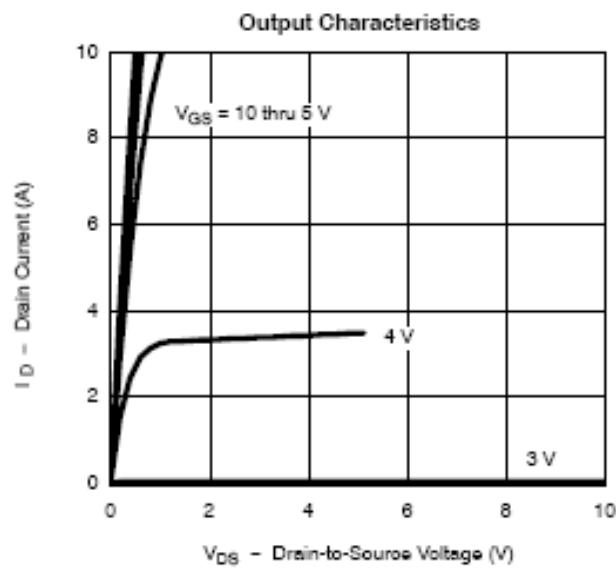
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, ID=250uA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , ID=250uA	1.0		3.0	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =1.0V			1	uA
		V _{DS} =30V, V _{GS} =0.0V T _J =55°C			10	
On-State Drain Current	I _{D(on)}	V _{DS} ≥4.5V, V _{GS} =10V	6			A
		V _{DS} ≥4.5V, V _{GS} =4.5V	4			
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} = 10V, ID=5.5A		0.050	0.058	Ω
		V _{GS} = 4.5V, ID=4.0A		0.078	0.098	
Forward Transconductance	g _{fs}	V _{DS} =4.5V, ID=2.5A		4.6		S
Diode Forward Voltage	V _{SD}	I _S =1.25A, V _{GS} =0V		0.82	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V V _{GS} =10V ID=2.5		4.5	10	nC
Gate-Source Charge	Q _{gs}			0.8		
Gate-Drain Charge	Q _{gd}			1.0		
Input Capacitance	C _{iss}	V _{DS} =15V V _{GS} =0V f=1MHz		240		pF
Output Capacitance	C _{oss}			110		
Reverse Transfer Capacitance	C _{rss}			17		
Turn-On Time	t _{d(on)}	V _{DD} =15 R _L =15 ID=1.0A, V _{GEN} =10 R _G =6Ω		8	20	ns
	t _r			12	30	
Turn-Off Time	t _{d(off)}			17	35	
	t _f			8	20	



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TYPICAL CHARACTERISTICS

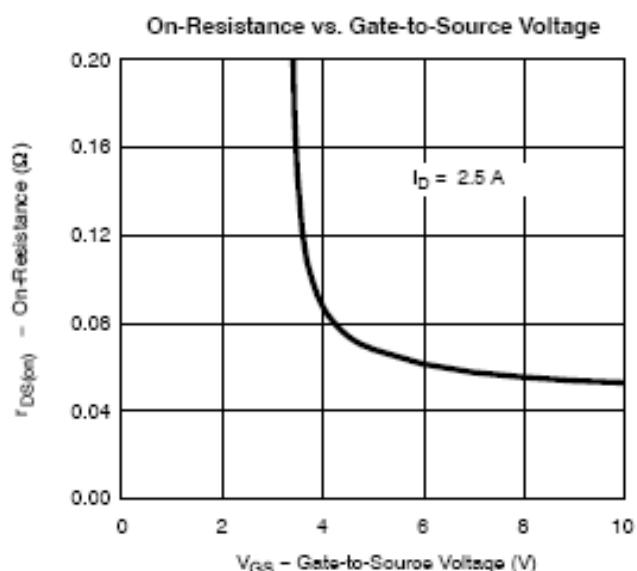
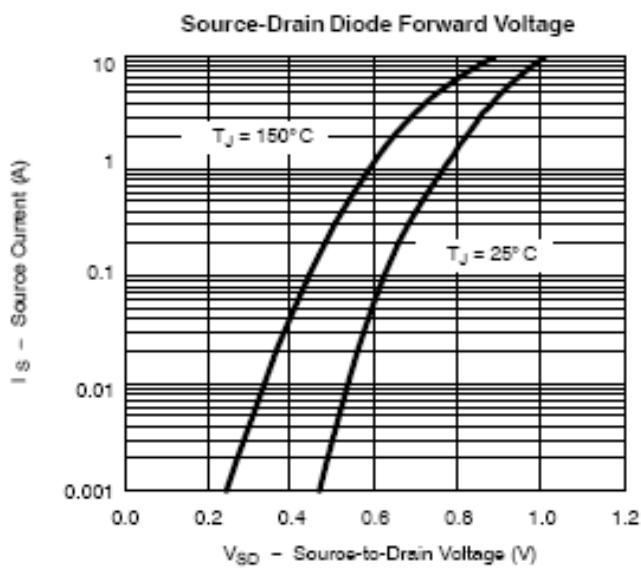
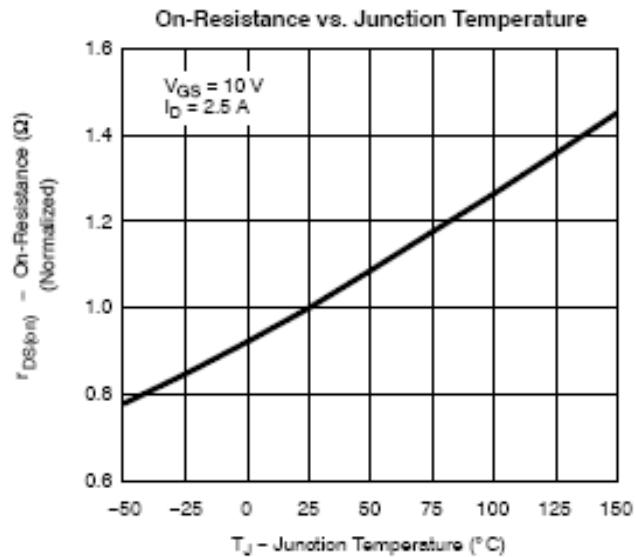
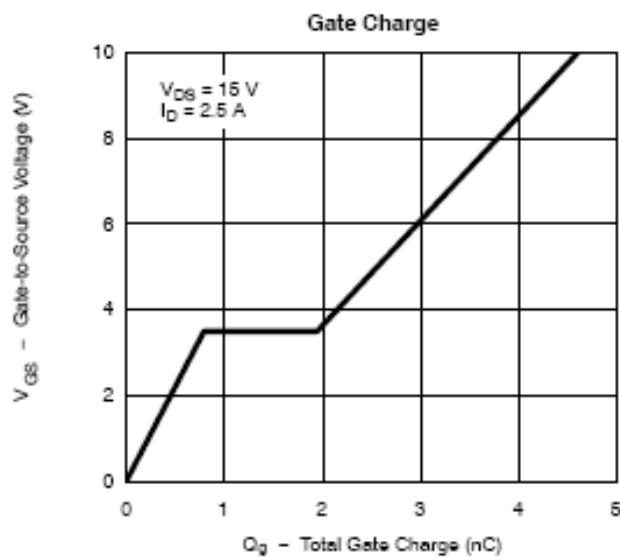




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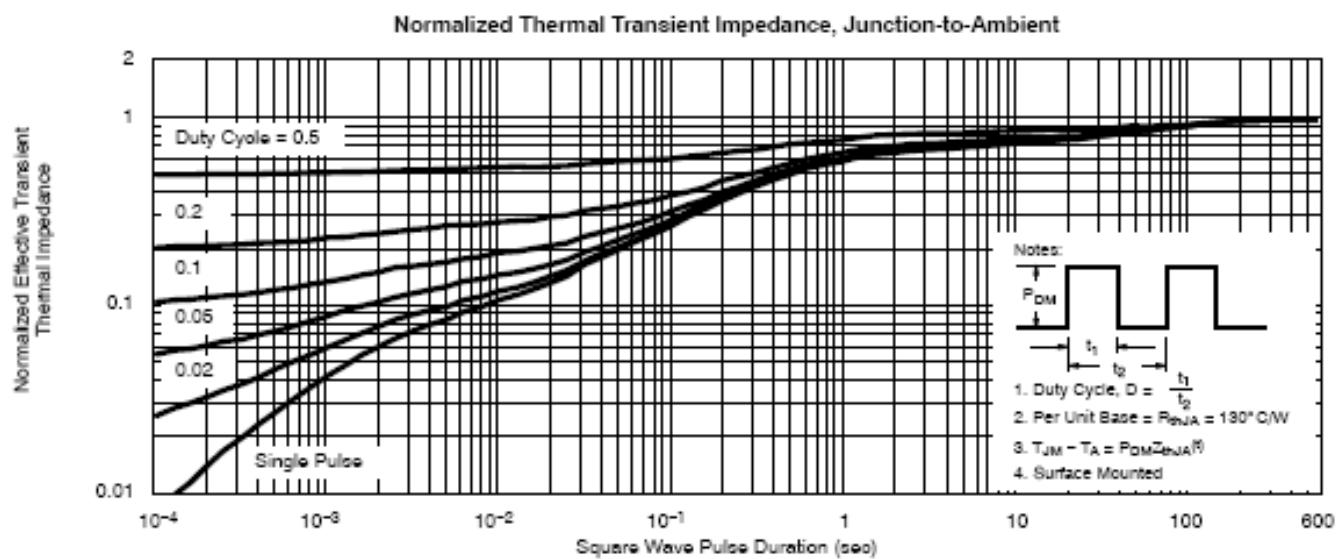
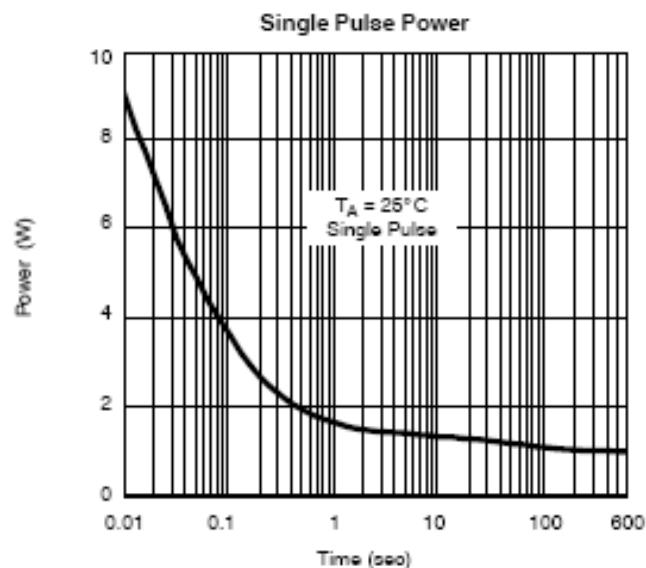
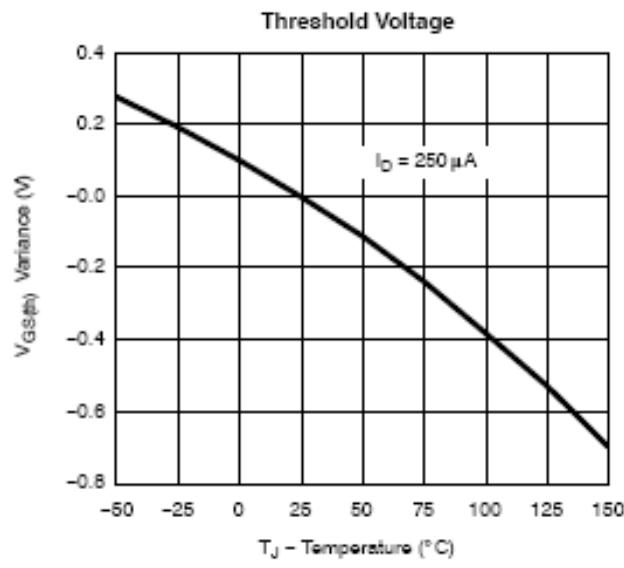




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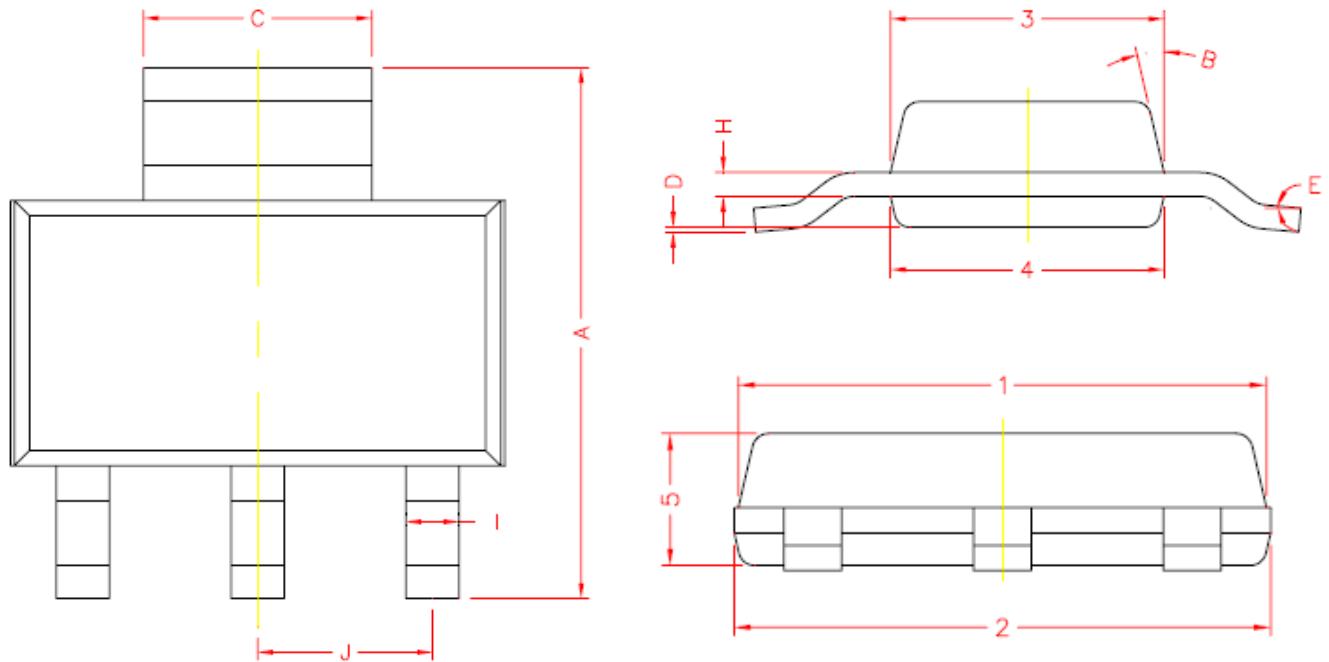




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SOT-233 PACKAGE OUTLINE



REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	6.70	7.30
C	2.90	3.10
D	0.02	0.10
E	0°	10°
I	0.60	0.80
H	0.25	0.35
B	13° TYP.	
J	2.30 REF.	
1	6.30	6.70
2	6.30	6.70
3	3.30	3.70
4	3.30	3.70
5	1.40	1.80



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