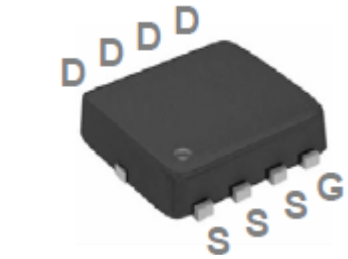
SPN8668
N-Channel Enhancement Mode MOSFET

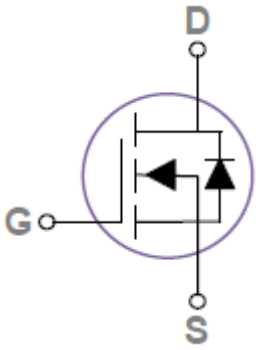
DESCRIPTION
The SPN8668 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high efficiency and fast switching is required.

APPLICATIONS
- Motor Drive
- Power Tools
- LED Lighting

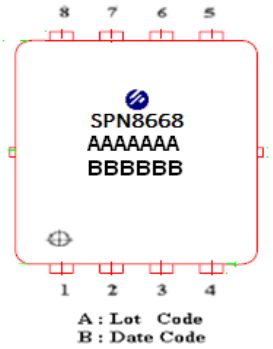
FEATURES
- 60V/80A,$R_{DS(ON)}$=21mΩ@V_{GS}=10V
- 60V/80A,$R_{DS(ON)}$=24mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x3-8L package design

PIN CONFIGURATION(PPAK3x3-8L)





PART MARKING



SPN8668
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8668DN8RGB	PPAK3x3-8L	SPN8668

※ SPN8668DN8RGB : 13" Tape Reel ; Pb – Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_C=25℃	I_D	80	A
	T_C=100℃		57	
Pulsed Drain Current		I_{DM}	132	A
Continuous Source Current(Diode Conduction)		I_S	33	A
Power Dissipation	T_A=25℃	P_D	7	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	62	℃/W
Thermal Resistance-Junction to Case		$R_{\theta JC}$	2.8	℃/W

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=25uA	1.2	1.8	2.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V, T_J=25℃			1	uA
		V_{DS}=48V,V_{GS}=0V, T_J=125℃			10	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=15A		17	21	mΩ
		V_{GS}=4.5V, I_D=8A		20	24	
Forward Transconductance	gfs	V_{DS}=10V, I_D=10A		9		S
Diode Forward Voltage	V_{SD}	I_F=1A,V_{GS}=0V			1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=30V,V_{GS}=10V, I_D=15A		28	42	nC
Gate-Source Charge	Q_{gs}			3.5	7	
Gate-Drain Charge	Q_{gd}			6.5	10	
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=20V, F=1MHz		1680	2440	pF
Output Capacitance	C_{oss}			115	170	
Reverse Transfer Capacitance	C_{rss}			85	125	
Turn-On Time	$t_{d(on)}$	(V_{DD}=30V,I_D=-1A, V_{GEN}=10V,R_G=6Ω)		7.2	14	ns
	t_r			38	72	
Turn-Off Time	$t_{d(off)}$			34	65	
	t_f			8.2	16	

TYPICAL CHARACTERISTICS

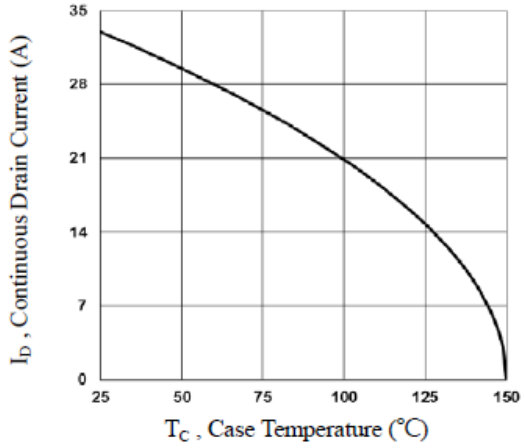


Fig.1 Continuous Drain Current vs. T_c

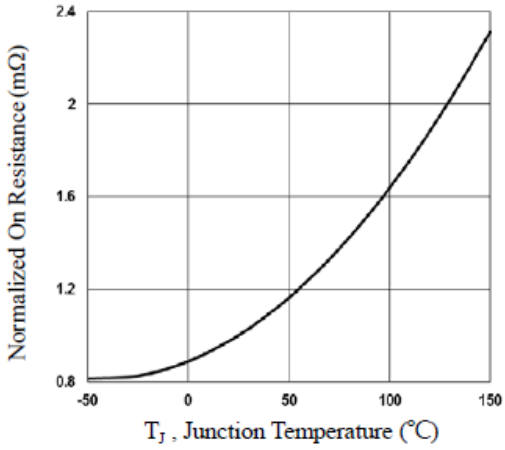


Fig.2 Normalized RDSON vs. T_J

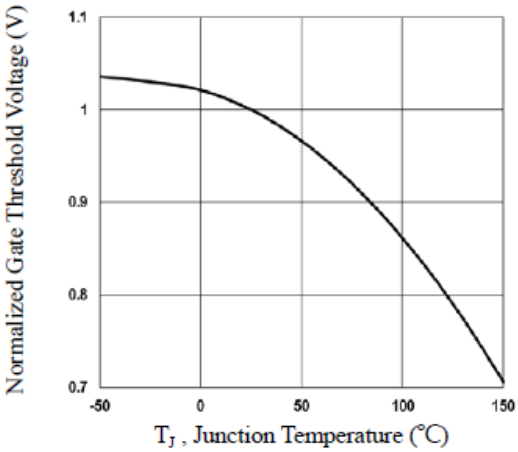


Fig.3 Normalized V_{th} vs. T_J

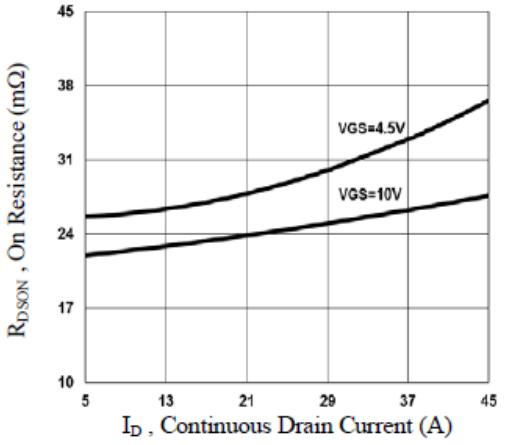


Fig.4 RDSON vs. Continuous Drain Current

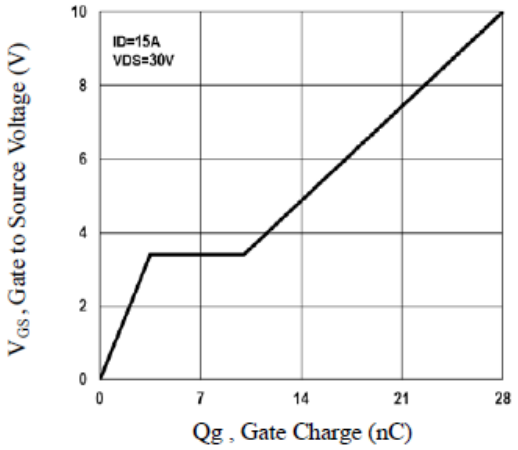


Fig.5 Gate Charge Waveform

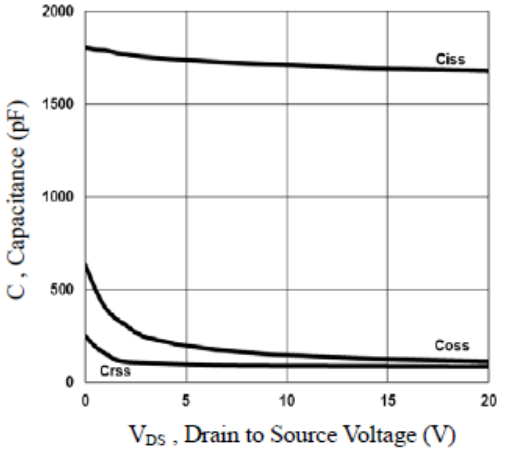


Fig.6 Capacitance Characteristics

TYPICAL CHARACTERISTICS

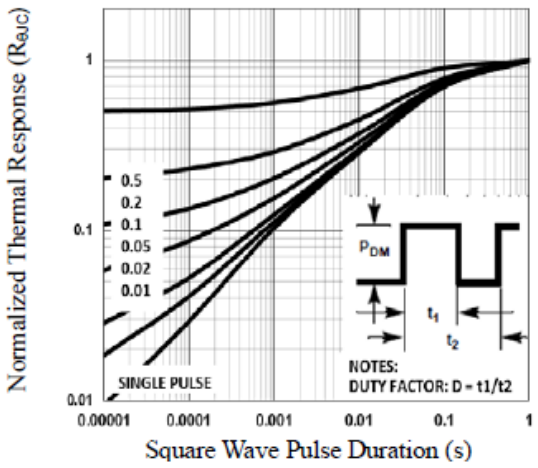


Fig.7 Normalized Transient Impedance

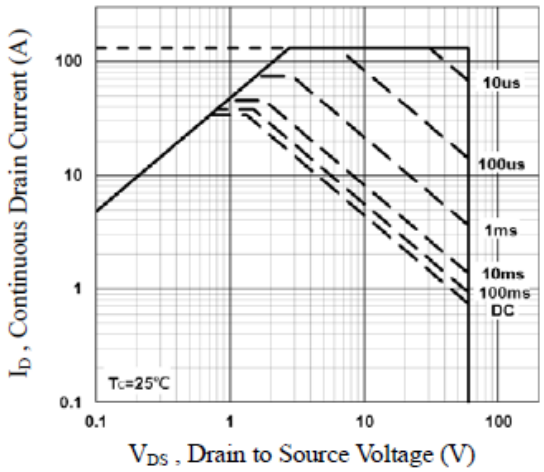


Fig.8 Maximum Safe Operation Area

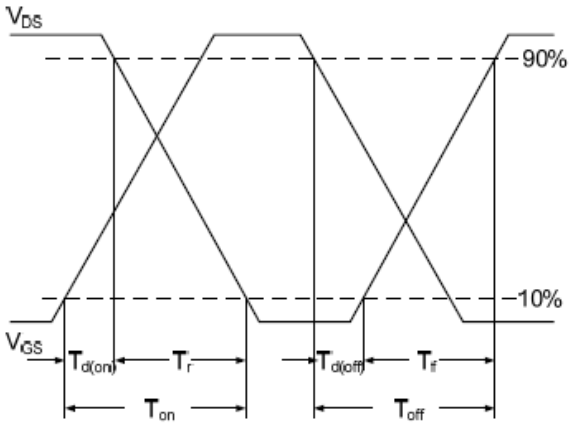


Fig.9 Switching Time Waveform

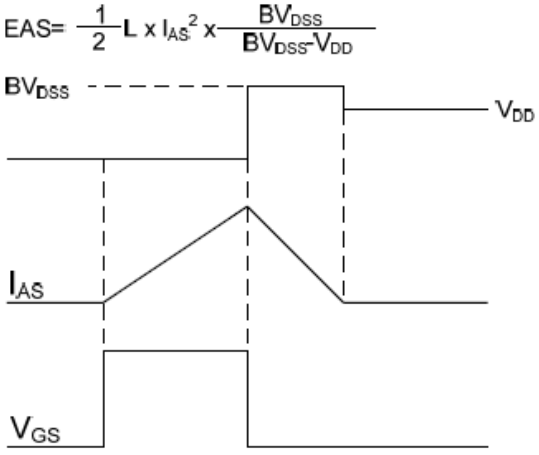
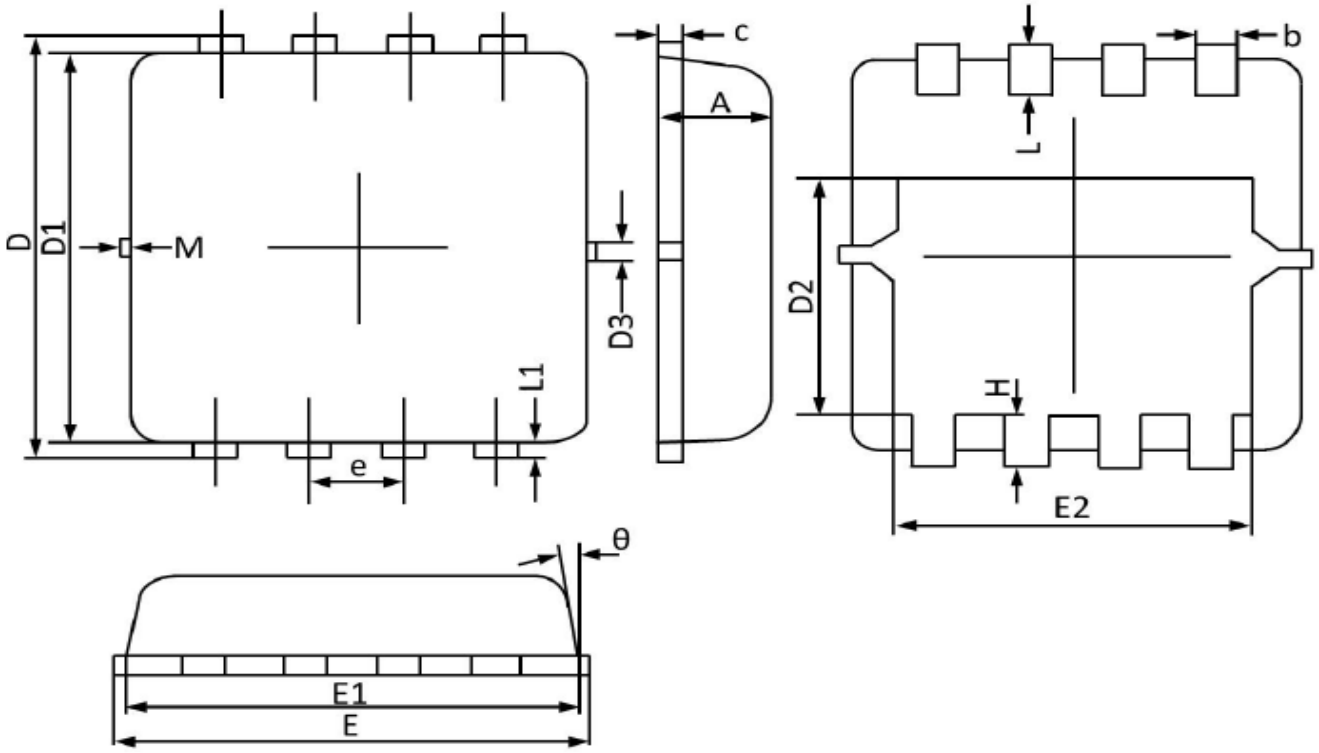


Fig.10 EAS Waveform

PPAK3x3-8L PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
b	0.250	0.350	0.010	0.013
c	0.100	0.250	0.004	0.009
D	3.250	3.450	0.128	0.135
D1	3.000	3.200	0.119	0.125
D2	1.780	1.980	0.070	0.077
D3	0.130 REF		0.005 REF	
E	3.200	3.400	0.126	0.133
E1	3.000	3.200	0.119	0.125
E2	2.390	2.590	0.094	0.102
e	0.650 BSC		0.026 BSC	
H	0.300	0.500	0.011	0.019
L	0.300	0.500	0.011	0.019
L1	0.130 REF		0.005 REF	
θ	0°	12°	0°	12°
M	0.150 REF		0.006 REF	

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