



SPP1305

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP1305 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

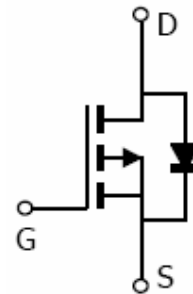
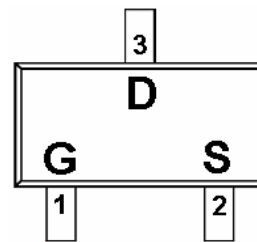
FEATURES

- ◆ -20V/-0.95A, $R_{DS(ON)}= 280m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-0.80A, $R_{DS(ON)}= 380m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-0.70A, $R_{DS(ON)}= 530m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low RDS (ON)
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-323 (SC-70) package design

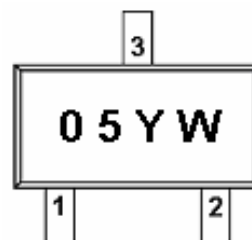
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (SOT-323 ; SC-70)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP1305S32RG	SOT-323	05YW

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPP1305S32RG : Tape Reel ; Pb – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-20	V	
Gate –Source Voltage	V _{GSS}	±12	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-1.0	A
		TA=70°C	-0.7	
Pulsed Drain Current	I _{DM}	-3	A	
Continuous Source Current(Diode Conduction)	I _S	-0.28	A	
Power Dissipation	P _D	TA=25°C	0.33	W
		TA=70°C	0.21	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	105	°C/W	



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ELECTRICAL CHARACTERISTICS

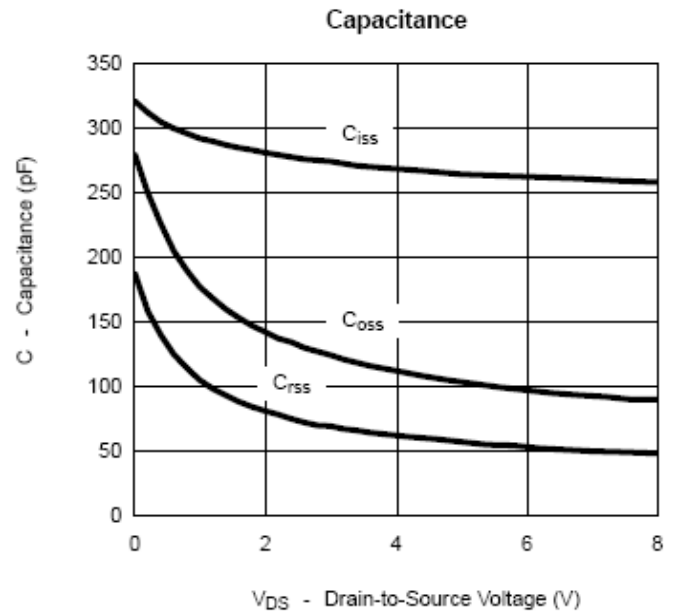
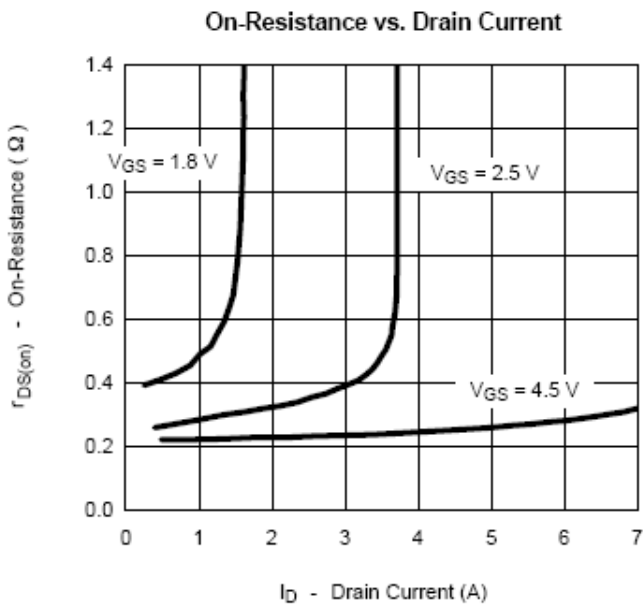
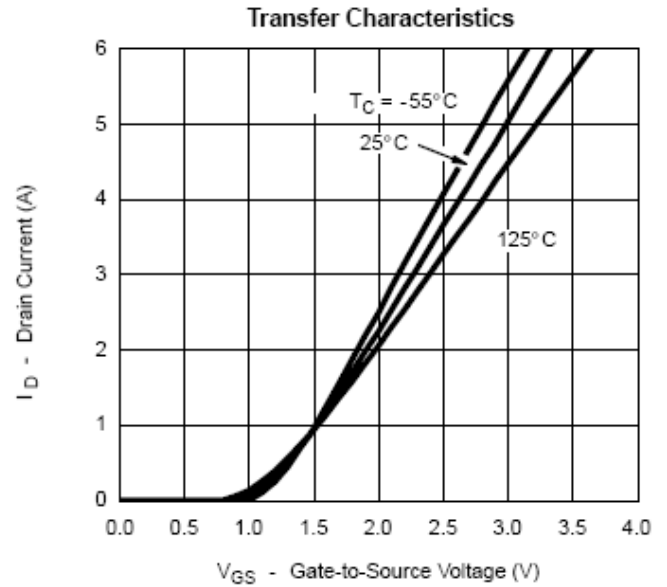
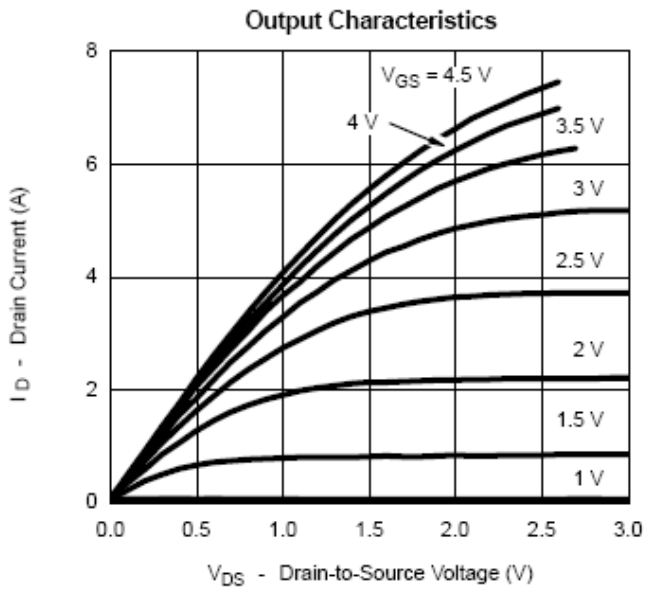
(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.5		-1.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	uA
		V _{DS} =-20V, V _{GS} =0V T _J =55°C			-5	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-6			A
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =-4.5V, I _D =-0.95A		0.22	0.28	Ω
		V _{GS} =-2.5V, I _D =-0.80A		0.30	0.38	
		V _{GS} =-1.8V, I _D =-0.70A		0.42	0.53	
Forward Transconductance	g _{fs}	V _{DS} =-5V, I _D =-1.0A		3.5		S
Diode Forward Voltage	V _{SD}	I _S =-0.5A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-4V, V _{GS} =-4.5V I _D =-1.0A		3.0	4.2	nC
Gate-Source Charge	Q _{gs}			0.6		
Gate-Drain Charge	Q _{gd}			0.5		
Input Capacitance	C _{iss}	V _{DS} =-4V, V _{GS} =0V f=1MHz		320		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			25		
Turn-On Time	t _{d(on)}	V _{DD} =-4V, R _L =4Ω I _D =-1.0A, V _{GEN} =-4.5V R _G =6Ω		10	16	ns
	t _r			40	60	
Turn-Off Time	t _{d(off)}			18	25	
	t _f			15	20	



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TYPICAL CHARACTERISTICS

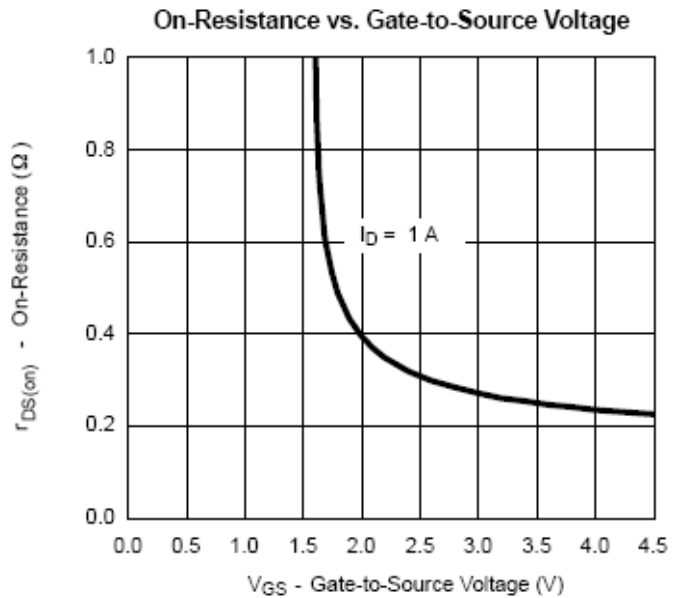
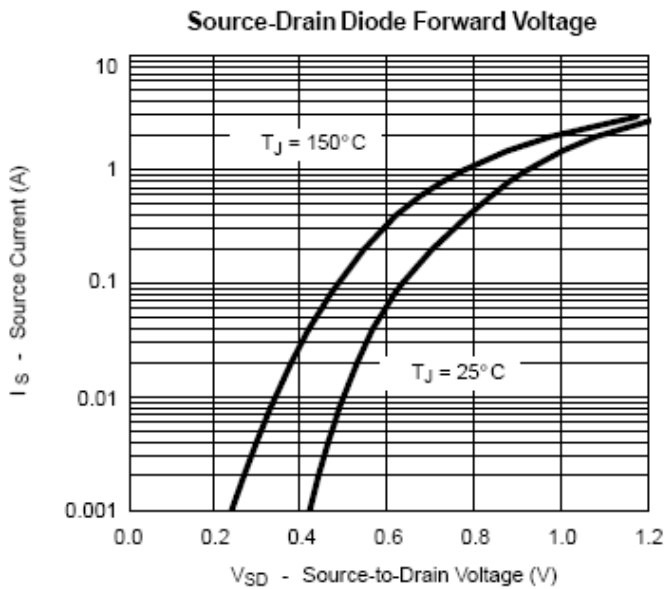
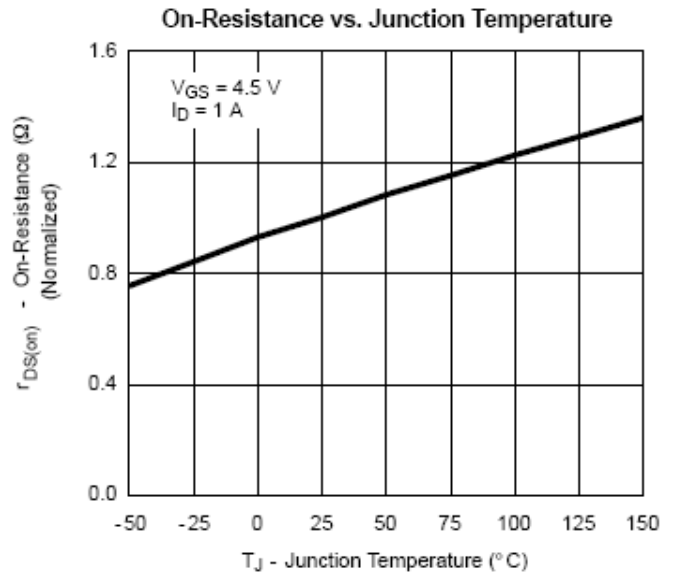
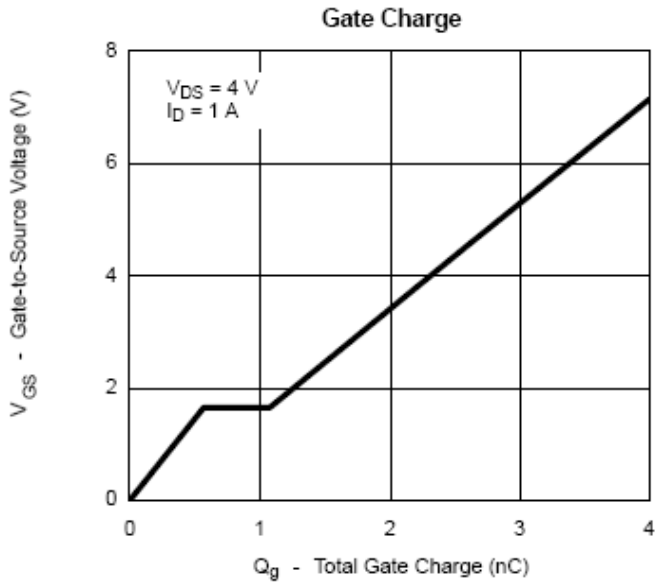




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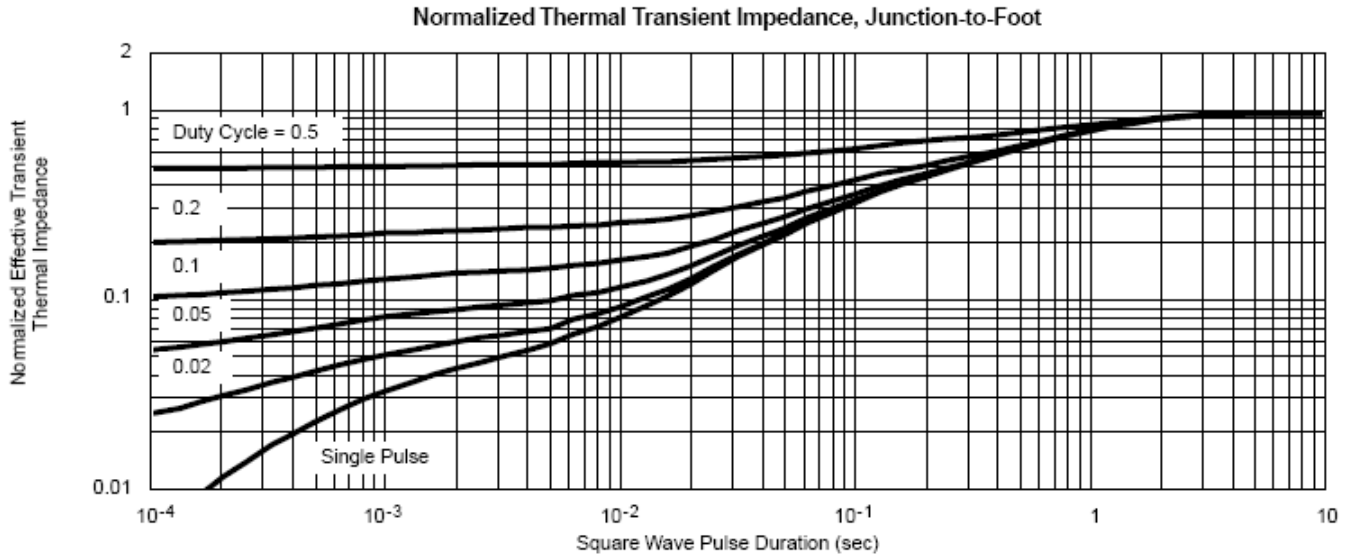
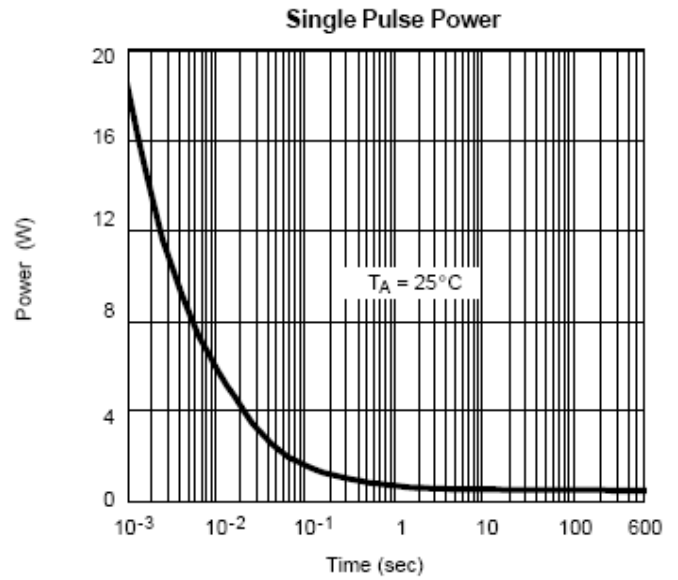
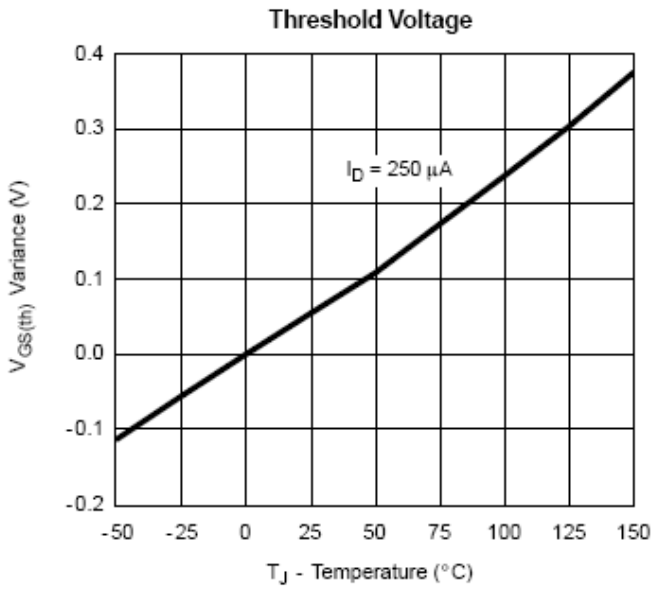
TYPICAL CHARACTERISTICS





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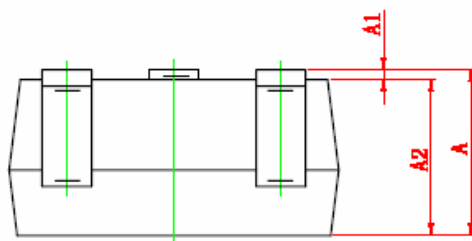
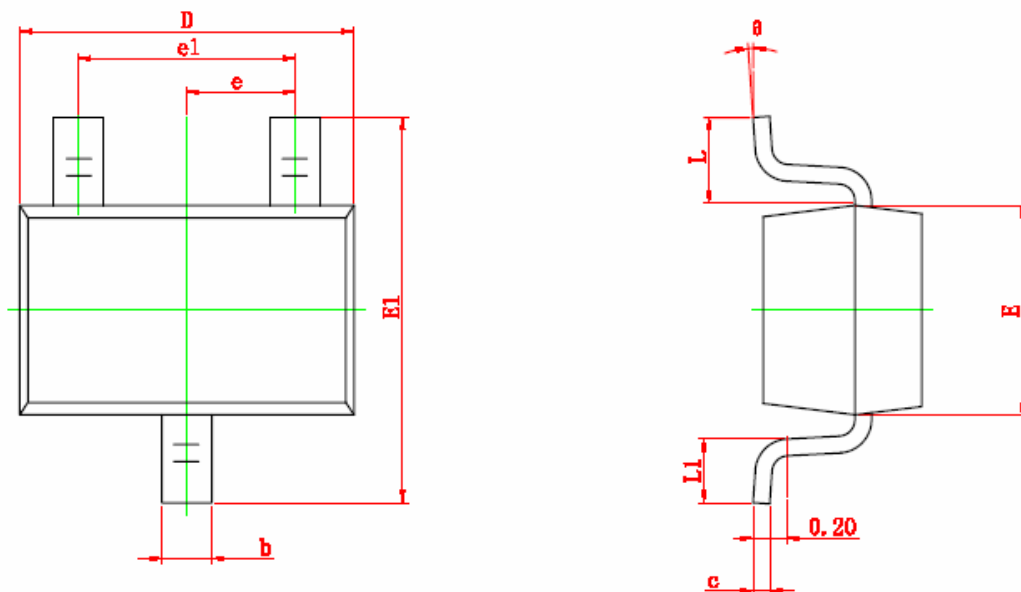




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SOT-323 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°



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