



SPP3421

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3421 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

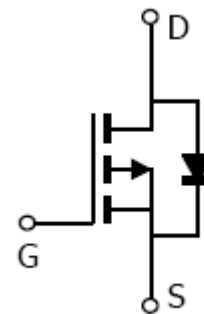
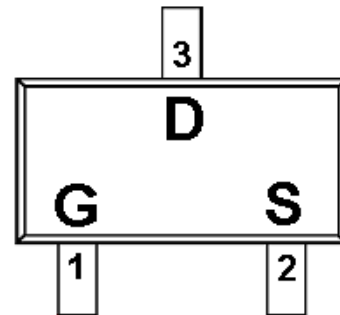
FEATURES

- ◆ -60V/-5A, $R_{DS(ON)}=150m\Omega@V_{GS}=-10V$
- ◆ -60V/-2.5A, $R_{DS(ON)}=185m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

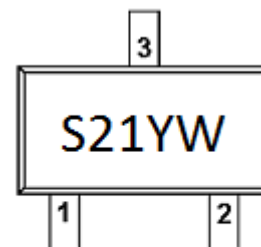
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOT-23)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

| Pin | Symbol | Description |
|-----|--------|-------------|
| 1 | G | Gate |
| 2 | S | Source |
| 3 | D | Drain |

ORDERING INFORMATION

| Part Number | Package | Part Marking |
|---------------|---------|--------------|
| SPP3421S23RGB | SOT-23 | S21YW |

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP3421S23RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Typical | Unit | |
|---|------------------|---------|------|---|
| Drain-Source Voltage | V _{DSS} | -60 | V | |
| Gate –Source Voltage | V _{GSS} | ±20 | V | |
| Continuous Drain Current(T _J =150°C) | I _D | TA=25°C | -5 | A |
| | | TA=70°C | -3.5 | |
| Pulsed Drain Current | I _{DM} | -12 | A | |
| Continuous Source Current(Diode Conduction) | I _S | -1.25 | A | |
| Power Dissipation | P _D | TA=25°C | 1.25 | W |
| | | TA=70°C | 0.8 | |
| Operating Junction Temperature | T _J | 150 | °C | |
| Storage Temperature Range | T _{STG} | -55/150 | °C | |
| Thermal Resistance-Junction to Ambient | R _{θJA} | 100 | °C/W | |



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

| Parameter | Symbol | Conditions | Min. | Typ | Max. | Unit | |
|---------------------------------|---------------|--|------|------|-----------|------|--|
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=-250\mu A$ | -60 | | | V | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=-250\mu A$ | -1 | | -3 | | |
| Gate Leakage Current | I_{GSS} | $V_{DS}=0V, V_{GS}=\pm 20V$ | | | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=-48V, V_{GS}=0V$ | | | -1 | uA | |
| | | $V_{DS}=-48V, V_{GS}=0V$ $T_J=55^\circ C$ | | | -10 | | |
| On-State Drain Current | $I_{D(on)}$ | $V_{DS} \leq -5V, V_{GS}=-10V$ | | | -5 | A | |
| | | $V_{DS} \leq -5V, V_{GS}=-4.5V$ | | | -2.5 | | |
| Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}=-10V, I_D=-5A$ | | 150 | 160 | mΩ | |
| | | $V_{GS}=-4.5V, I_D=-2.5A$ | | 185 | 200 | | |
| Forward Transconductance | g_{fs} | $V_{DS}=-10V, I_D=-1.7A$ | | 2.4 | | S | |
| Diode Forward Voltage | V_{SD} | $I_S=-1.25A, V_{GS}=0V$ | | -0.8 | -1.2 | V | |
| Dynamic | | | | | | | |
| Total Gate Charge | Q_g | $V_{DS}=-30V, V_{GS}=-10V$ $I_D=-2A$ | | 16 | | nC | |
| Gate-Source Charge | Q_{gs} | | | 8 | | | |
| Gate-Drain Charge | Q_{gd} | | | 3.0 | | | |
| Input Capacitance | C_{iss} | $V_{DS}=-30V, V_{GS}=0V$ $f=1MHz$ | | | 1200 | pF | |
| Output Capacitance | C_{oss} | | | 115 | | | |
| Reverse Transfer Capacitance | C_{rss} | | | 7 | | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}=-10V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-3V$ $R_G=2.5\Omega$ | | 9 | | ns | |
| | t_r | | | 109 | | | |
| Turn-Off Time | $t_{d(off)}$ | | | | 25 | | |
| | t_f | | | | 11 | | |



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TYPICAL CHARACTERISTICS

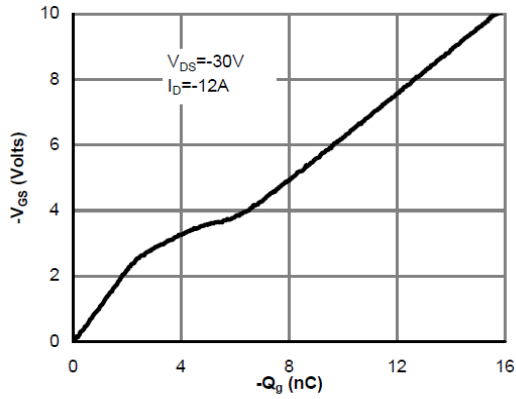


Figure 7: Gate-Charge Characteristics

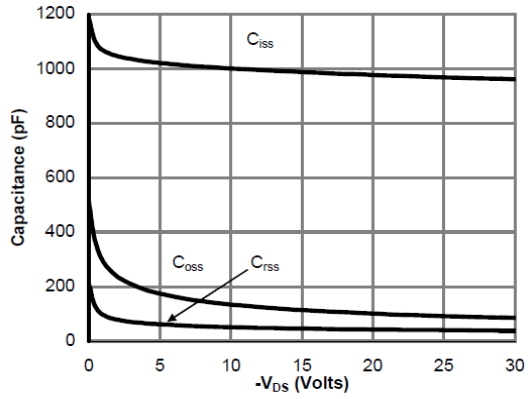


Figure 8: Capacitance Characteristics

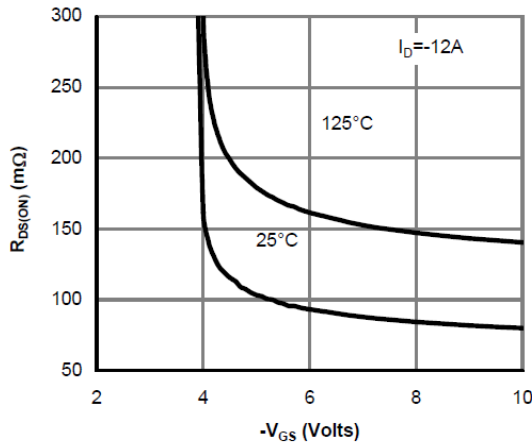


Figure 5: On-Resistance vs. Gate-Source Voltage

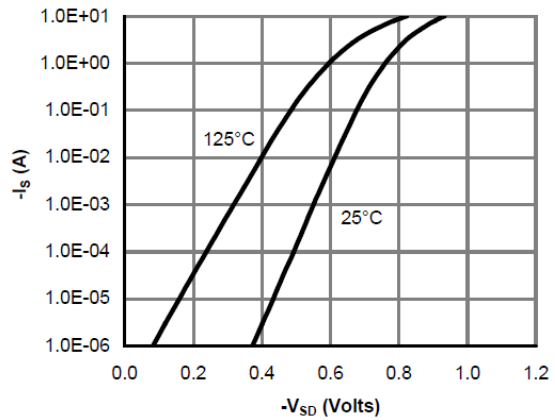


Figure 6: Body-Diode Characteristics

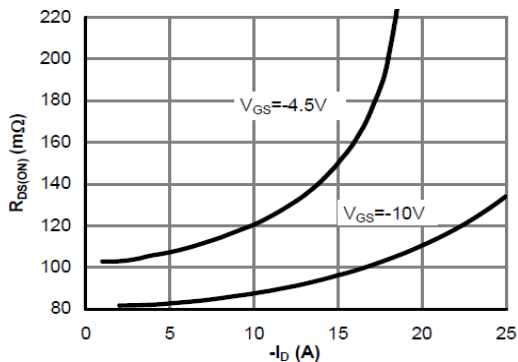


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

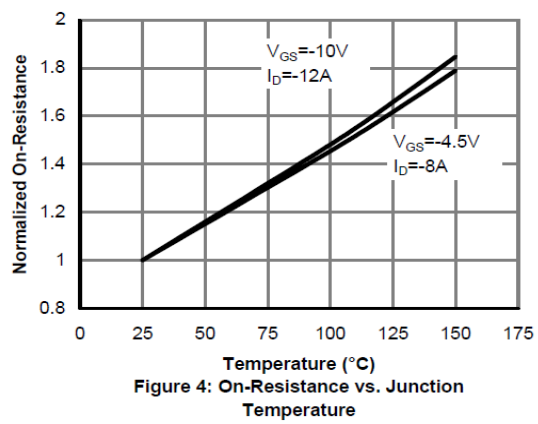


Figure 4: On-Resistance vs. Junction Temperature



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TYPICAL CHARACTERISTICS

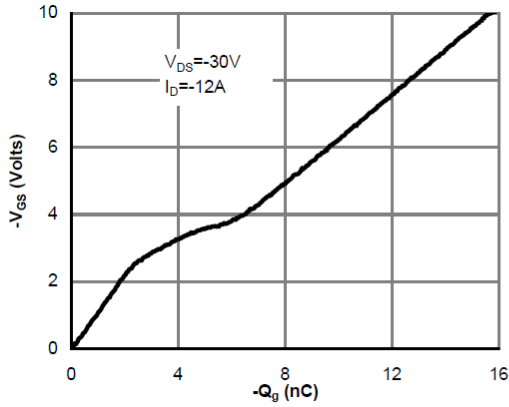


Figure 7: Gate-Charge Characteristics

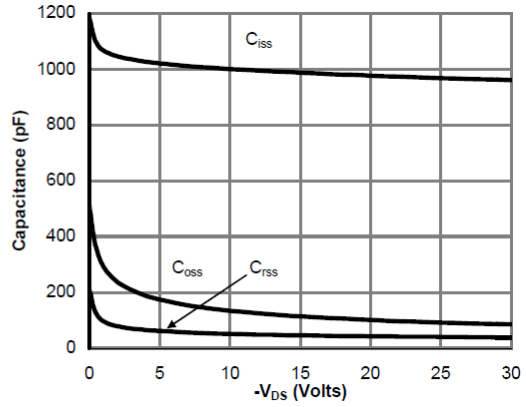


Figure 8: Capacitance Characteristics

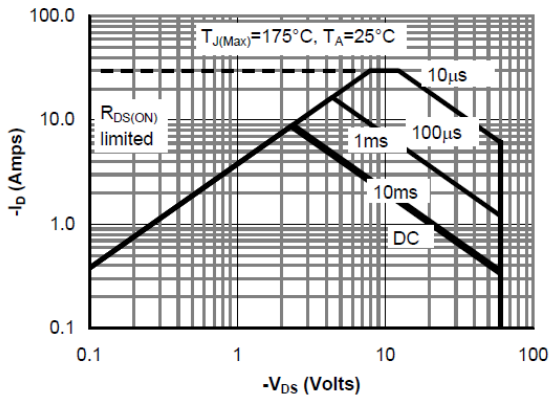


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

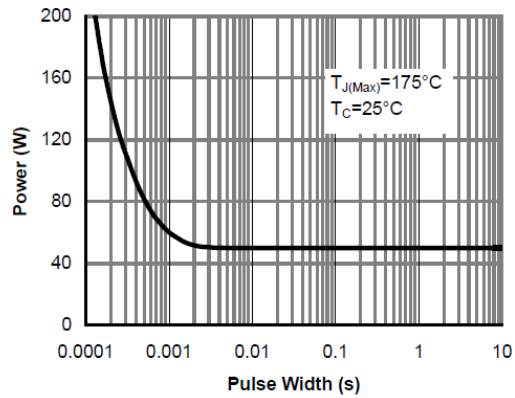


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

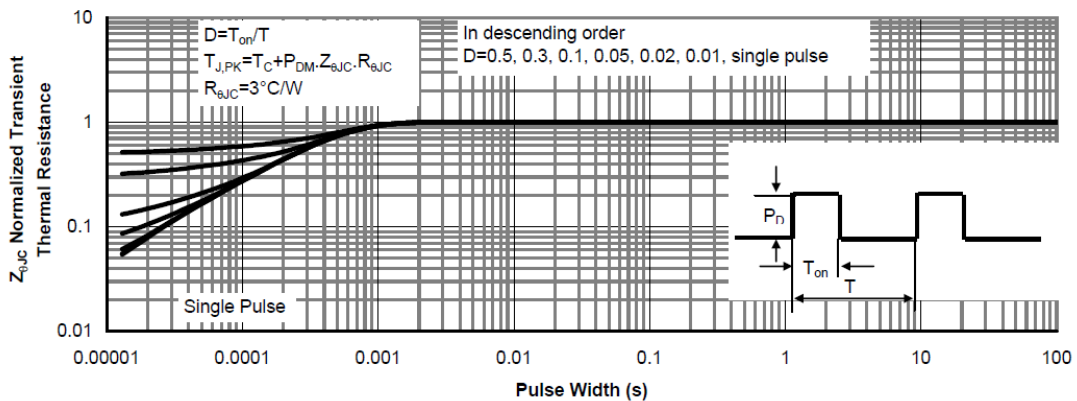


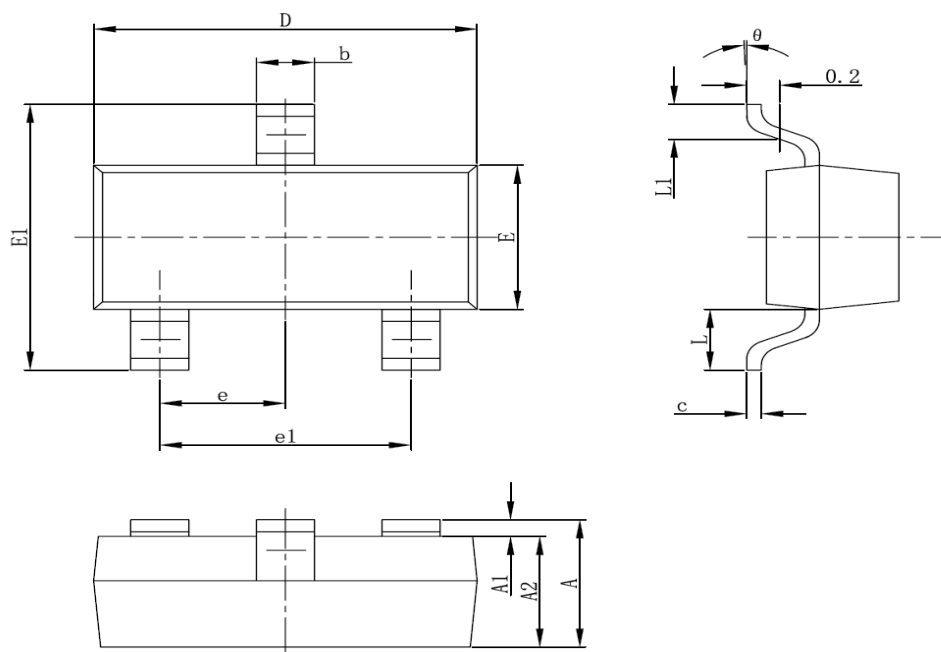
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



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SOT-23 PACKAGE OUTLINE



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.900 | 1.100 | 0.035 | 0.043 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.000 | 0.035 | 0.039 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.800 | 3.000 | 0.110 | 0.118 |
| E | 1.200 | 1.400 | 0.047 | 0.055 |
| E1 | 2.250 | 2.550 | 0.089 | 0.100 |
| e | 0.950TYP | | 0.037TYP | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.550REF | | 0.022REF | |
| L1 | 0.300 | 0.500 | 0.012 | 0.020 |
| theta | 0° | 8° | 0° | 8° |



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