



# SPP4435B P-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPP4435B is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

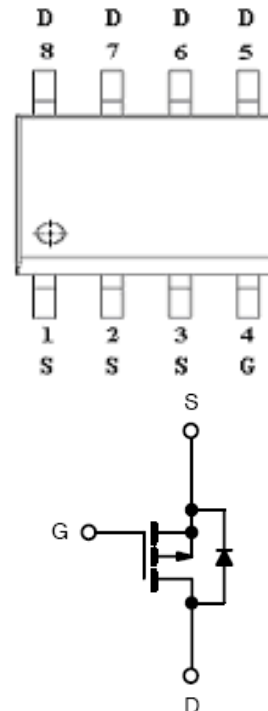
## FEATURES

- ◆ -30V/-9.2A, $R_{DS(ON)}=24m\Omega@V_{GS}=-10V$
- ◆ -30V/-7.0A, $R_{DS(ON)}=30m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

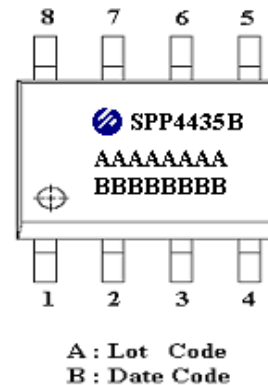
## APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

## PIN CONFIGURATION(SOP – 8P)



## PART MARKING





# SPP4435B

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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP4435BS8RGB	SOP- 8P	SPP4435B

※ SPP4435BS8RGB : 13" Tape Reel ; Pb – Free; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-30	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-10.0
		TA=70°C	-7.0
Pulsed Drain Current	I <sub>DM</sub>	-50	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-2.3	A
Power Dissipation	P <sub>D</sub>	TA=25°C	2.8
		TA=70°C	1.8
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	70	°C/W



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

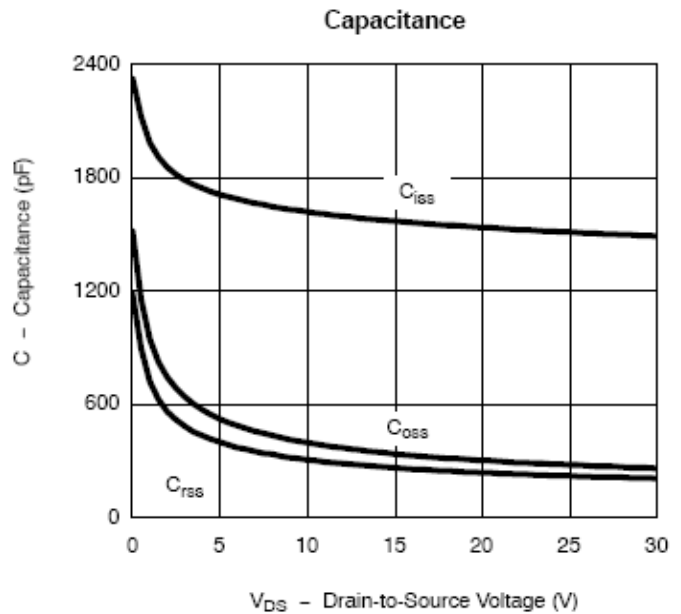
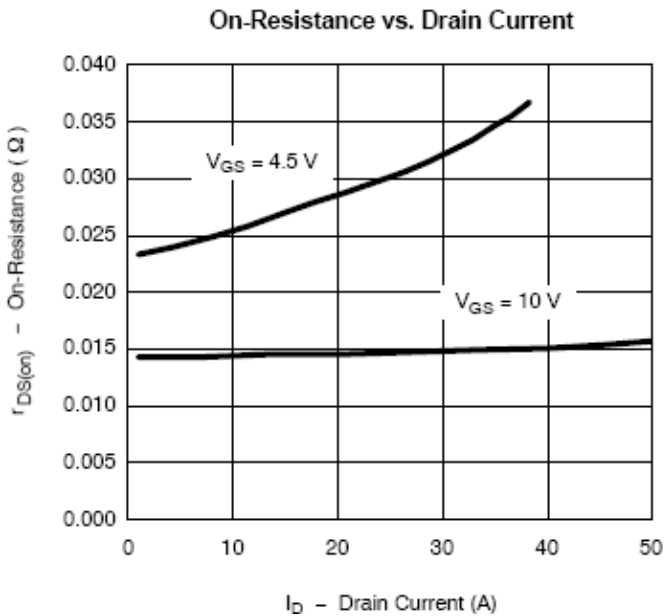
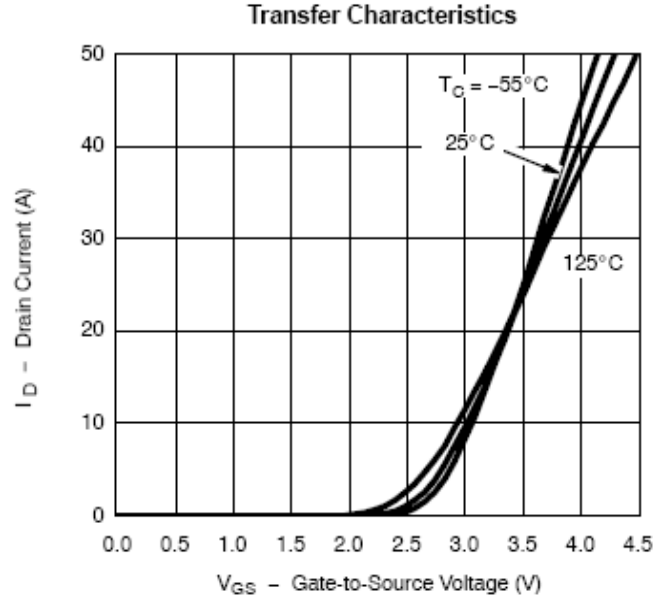
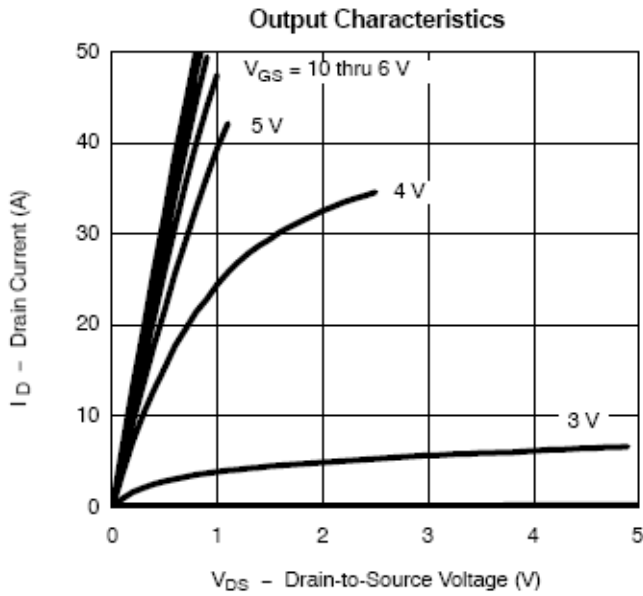
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7		-1.6	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-40			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-9.2A$		0.020	0.024	$\Omega$
		$V_{GS}=-4.5V, I_D=-7.0A$		0.025	0.030	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-9.0A$		24		S
Diode Forward Voltage	$V_{SD}$	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-9.0A$		20	30	nC
Gate-Source Charge	$Q_{gs}$			3.5		
Gate-Drain Charge	$Q_{gd}$			4.8		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		1850		pF
Output Capacitance	$C_{oss}$			450		
Reverse Transfer Capacitance	$C_{rss}$			335		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		20	30	nS
	$t_r$			20	30	
Turn-Off Time	$t_{d(off)}$			75	110	
	$t_f$			40	80	



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### TYPICAL CHARACTERISTICS

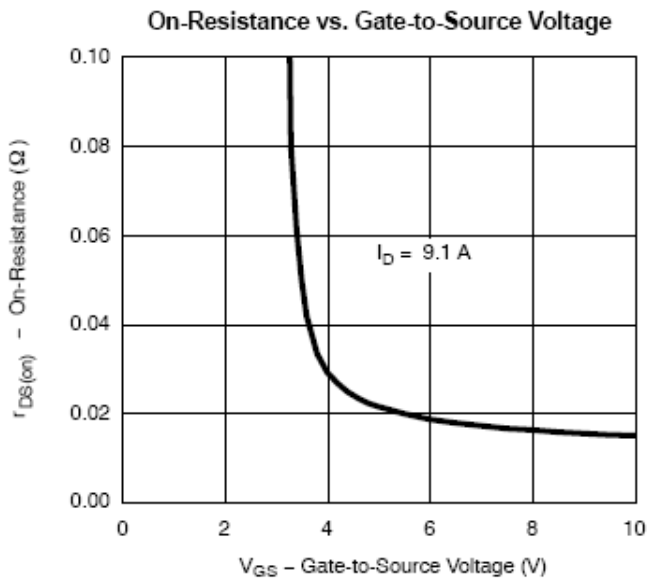
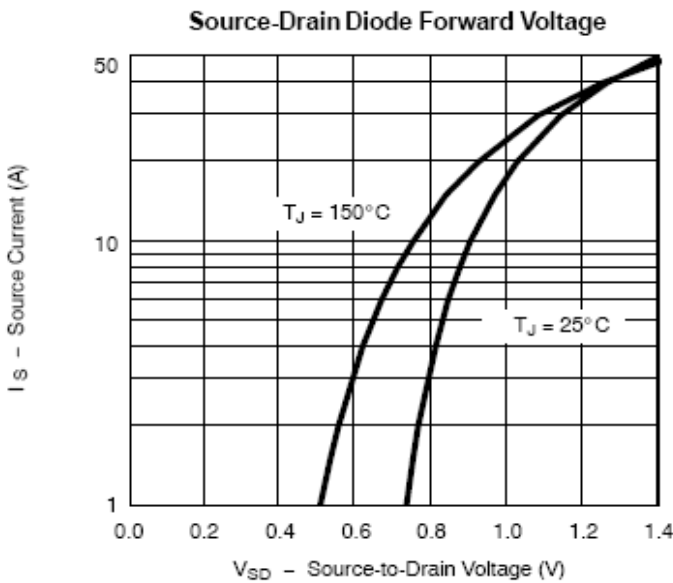
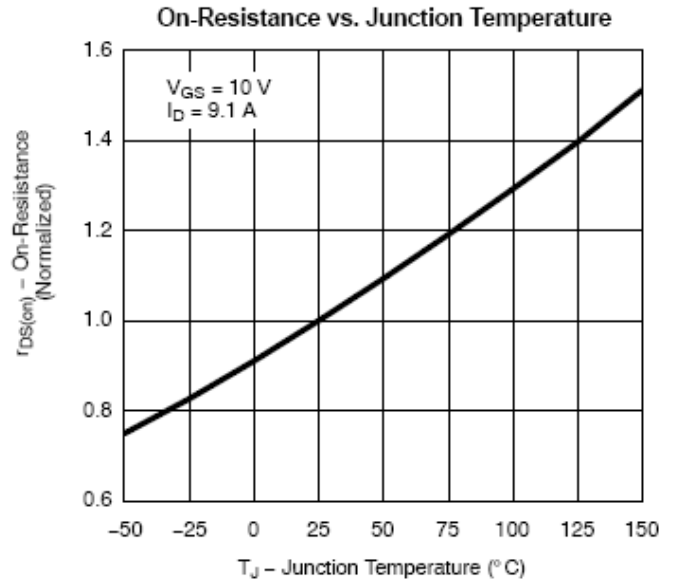
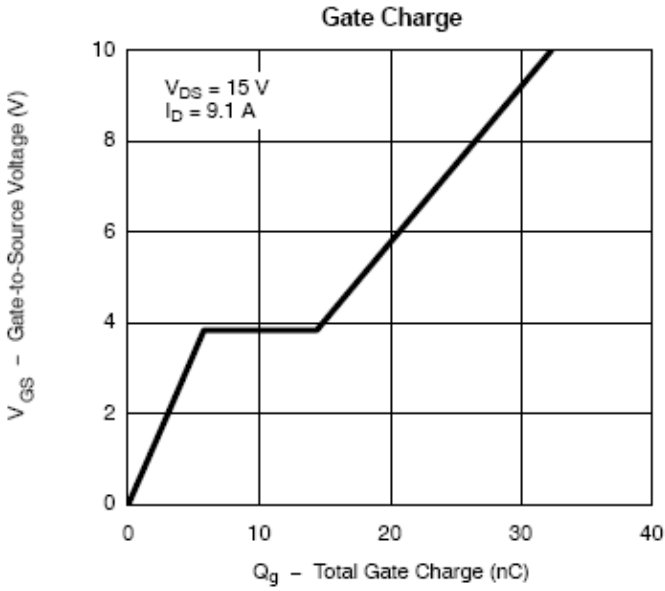




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### TYPICAL CHARACTERISTICS

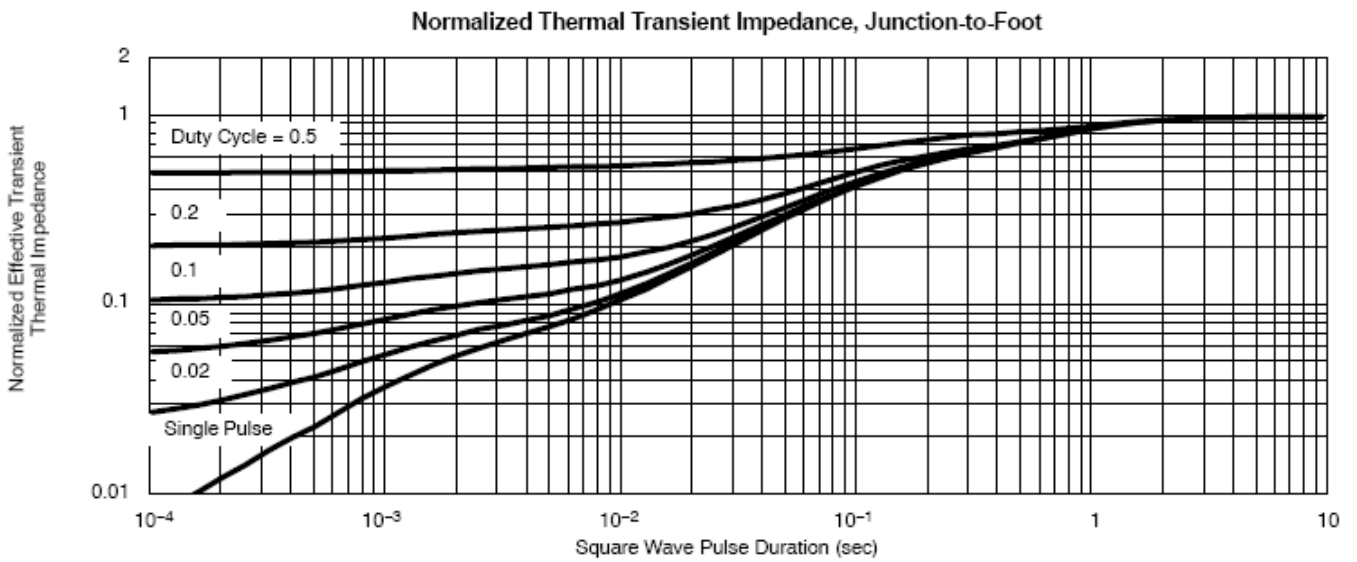
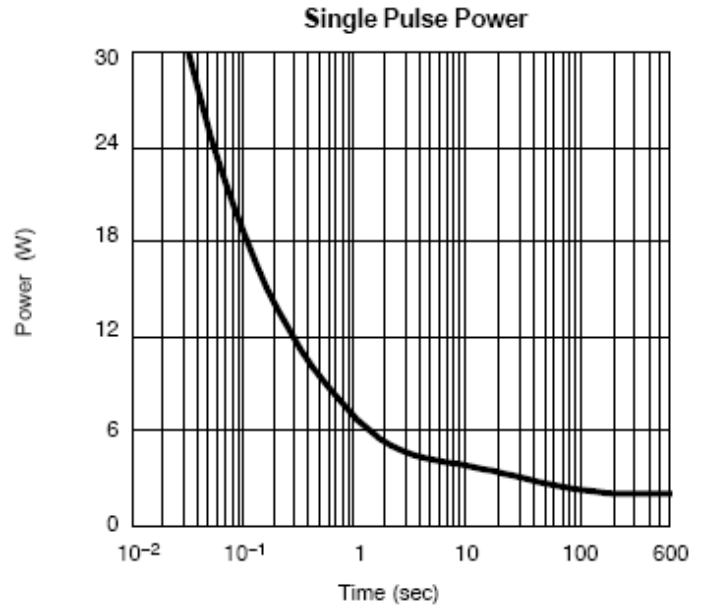
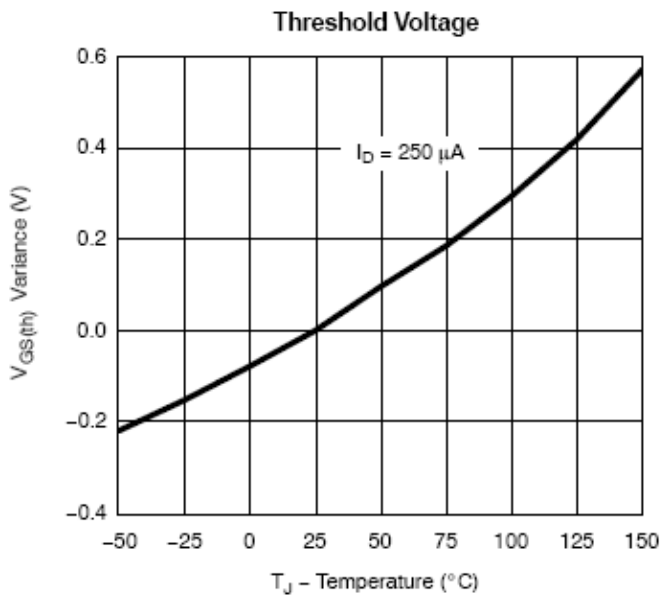




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### TYPICAL CHARACTERISTICS

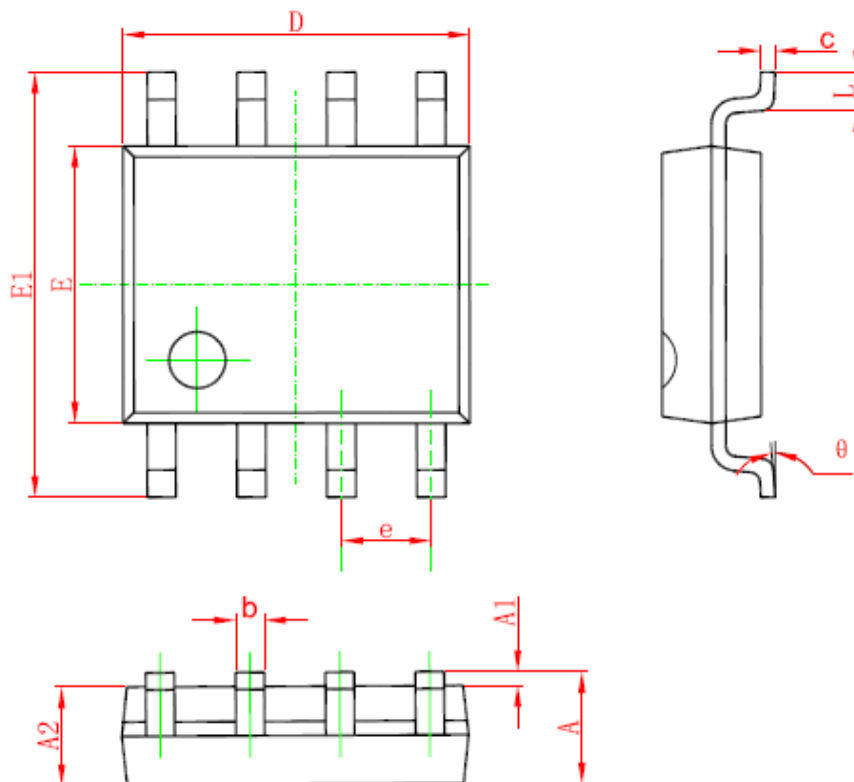




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### SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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