



# SPP9433W

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP9433W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

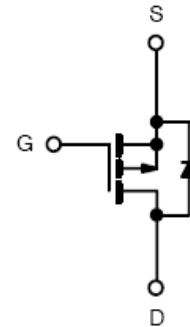
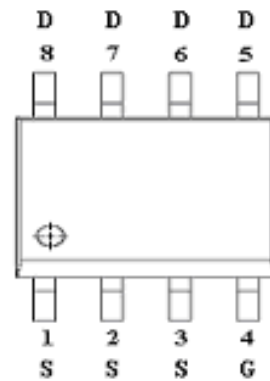
### FEATURES

- ◆ -30V/-6A,  $R_{DS(ON)} = 42m\Omega @ V_{GS} = -10V$
- ◆ -30V/-3 A,  $R_{DS(ON)} = 78m\Omega @ V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8P package design

### APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

### PIN CONFIGURATION(SOP – 8P)



### PART MARKING



A : Lot Code  
B : Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9433WS8RGB	SOP- 8P	SPP9433W

※ SPP9433WS8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-30	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-6	A
		TA=70°C	-4	
Pulsed Drain Current	I <sub>DM</sub>	-12	A	
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-6	A	
Power Dissipation	P <sub>D</sub>	2.08	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	60	°C/W	



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### ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1.0		-2.5	V	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA	
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-5		
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5V, V <sub>GS</sub> =-10V	-6			A	
Drain-Source On-Resistance	R <sub>DSON</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A		0.035	0.042	Ω	
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A		0.065	0.078		
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =-10.0V, I <sub>D</sub> =-6A		6		S	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-6A, V <sub>GS</sub> =0V			-1.2	V	
<b>Dynamic</b>							
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V I <sub>D</sub> =-6A		6.4		nC	
Gate-Source Charge	Q <sub>gs</sub>			2.7			
Gate-Drain Charge	Q <sub>gd</sub>			3.1			
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V f=1MHz		650		pF	
Output Capacitance	C <sub>oss</sub>			270			
Reverse Transfer Capacitance	C <sub>rss</sub>			104			
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-12V, I <sub>D</sub> =-5.0A, V <sub>GEN</sub> =-10V R <sub>G</sub> =3.3Ω		9		ns	
	t <sub>r</sub>			16			
Turn-Off Time	t <sub>d(off)</sub>				21		
	t <sub>f</sub>				22		



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### TYPICAL CHARACTERISTICS

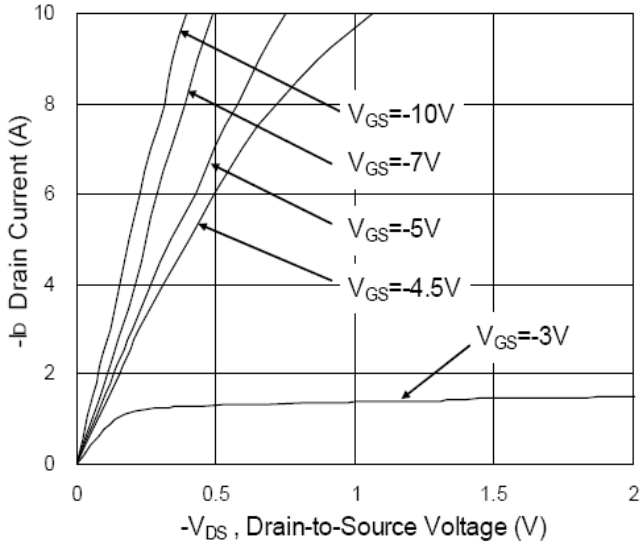


Fig. 1 Typical Output Characteristics

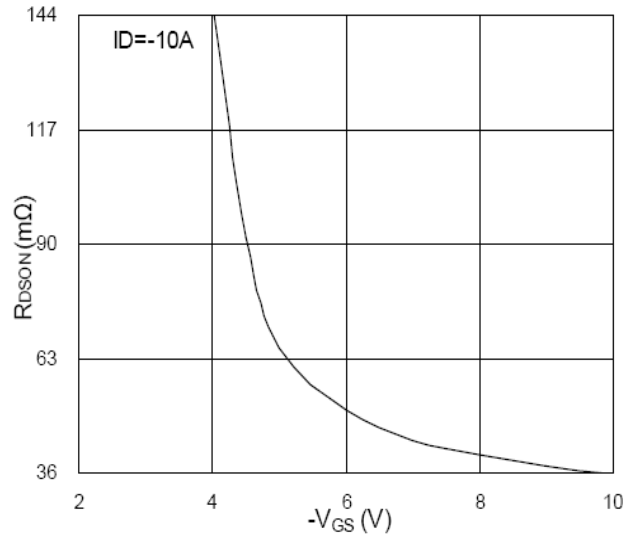


Fig. 2 On-Resistance vs. Gate Voltage

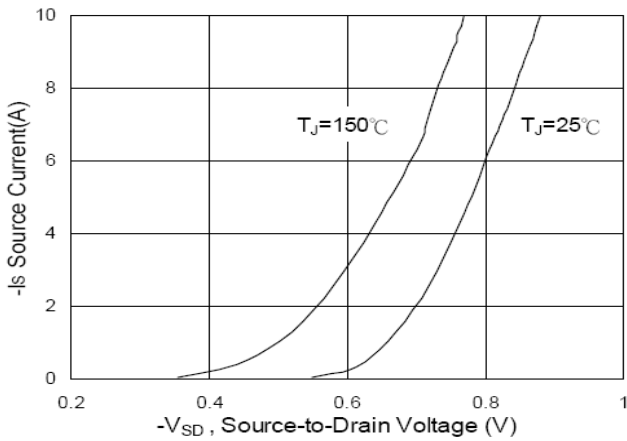


Fig. 3 Forward characteristics of Diodes

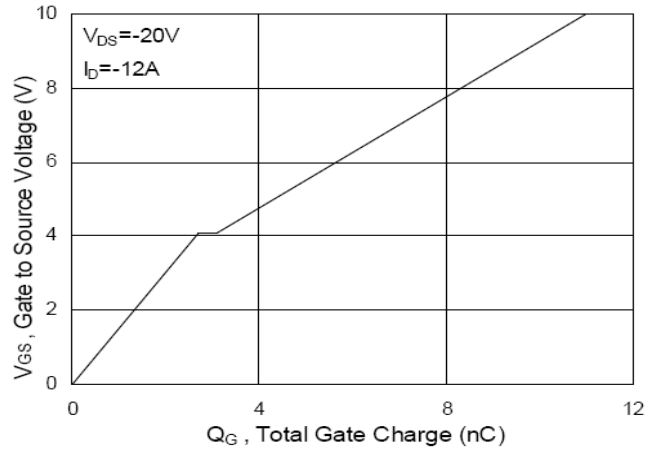


Fig. 4 Gate Charge Characteristics

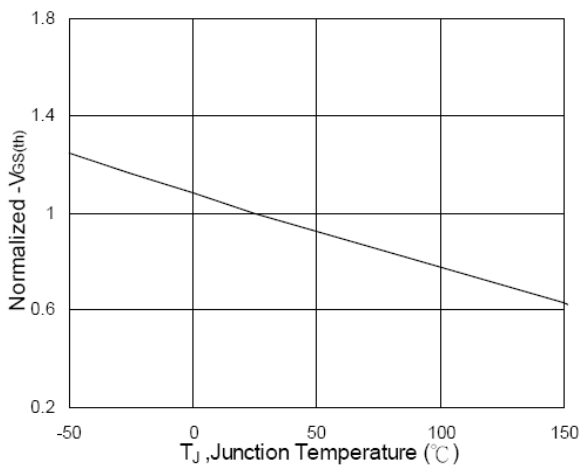


Fig. 5  $V_{GS}$  vs. Junction Temperature

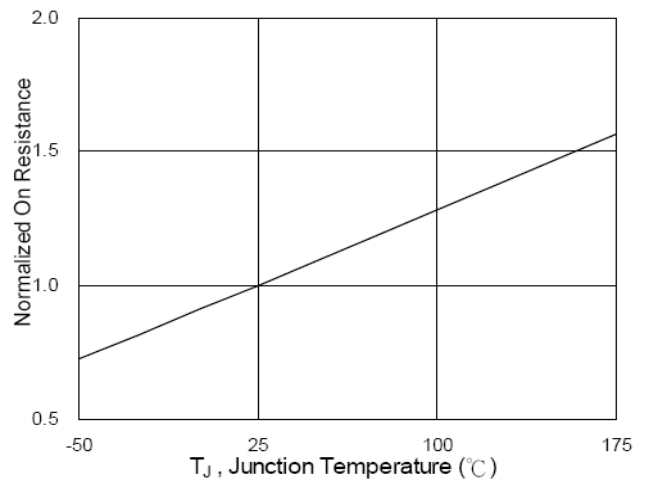


Fig. 6 On-Resistance vs Junction Temp



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## TYPICAL CHARACTERISTICS

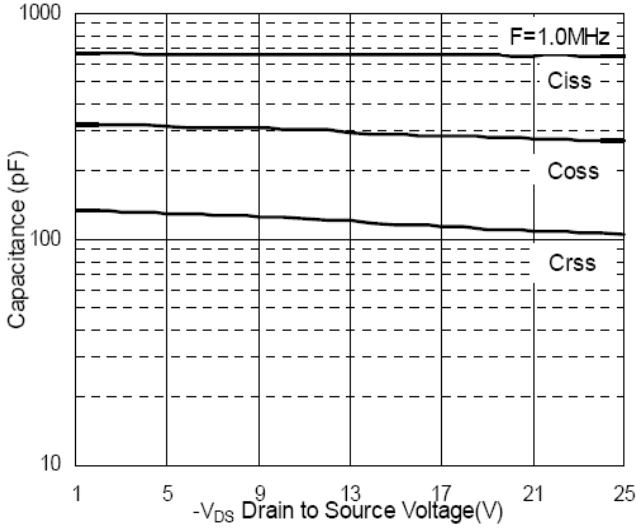


Fig. 7 Typical Capacitance Characteristics

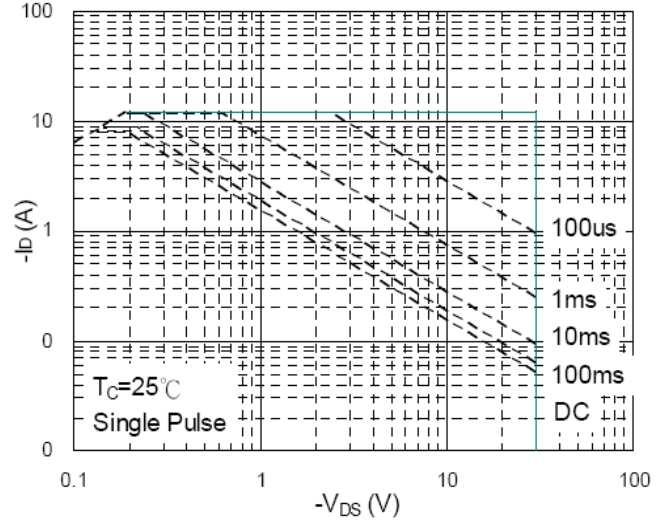


Fig. 8 Maximum Safe Operation Area

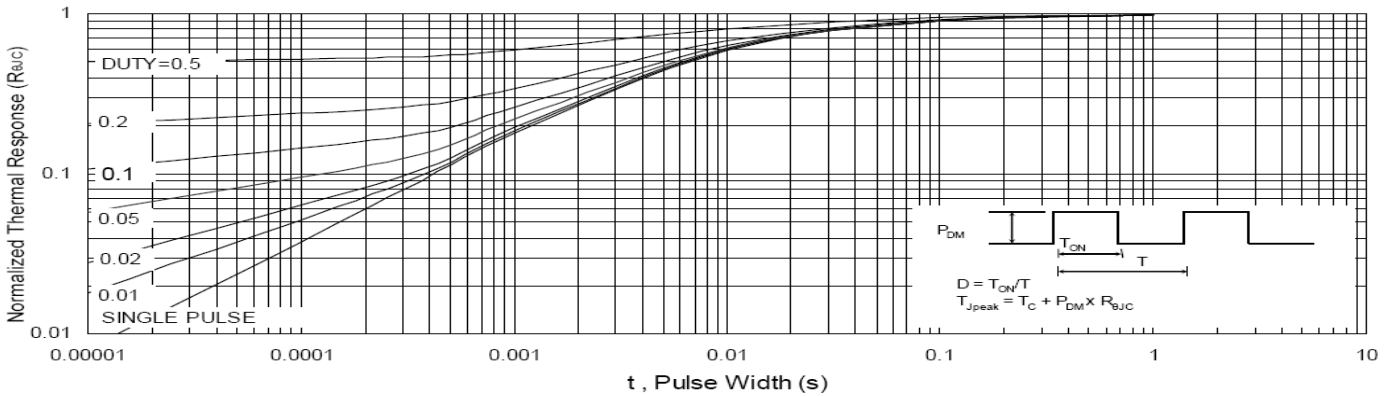


Fig. 9 Effective Transient Thermal Impedance

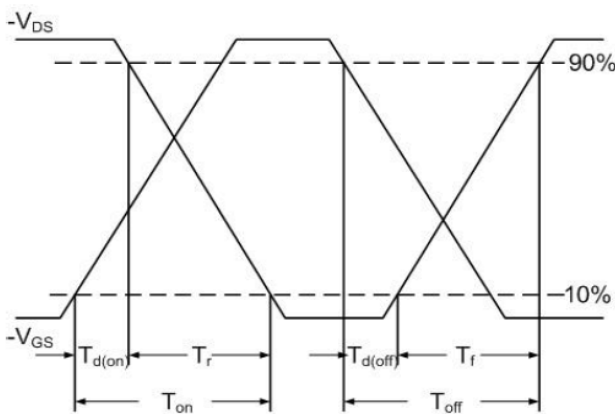


Fig. 10 Switching Time Waveform

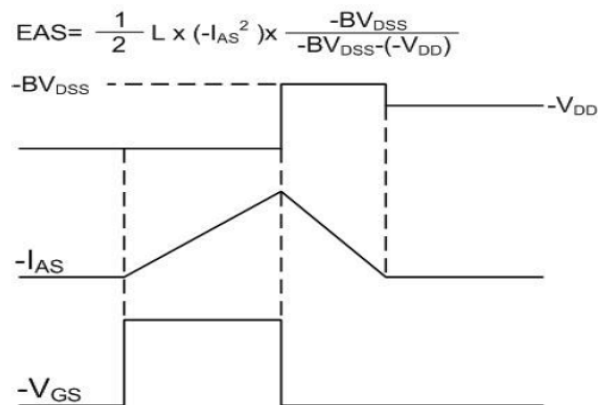


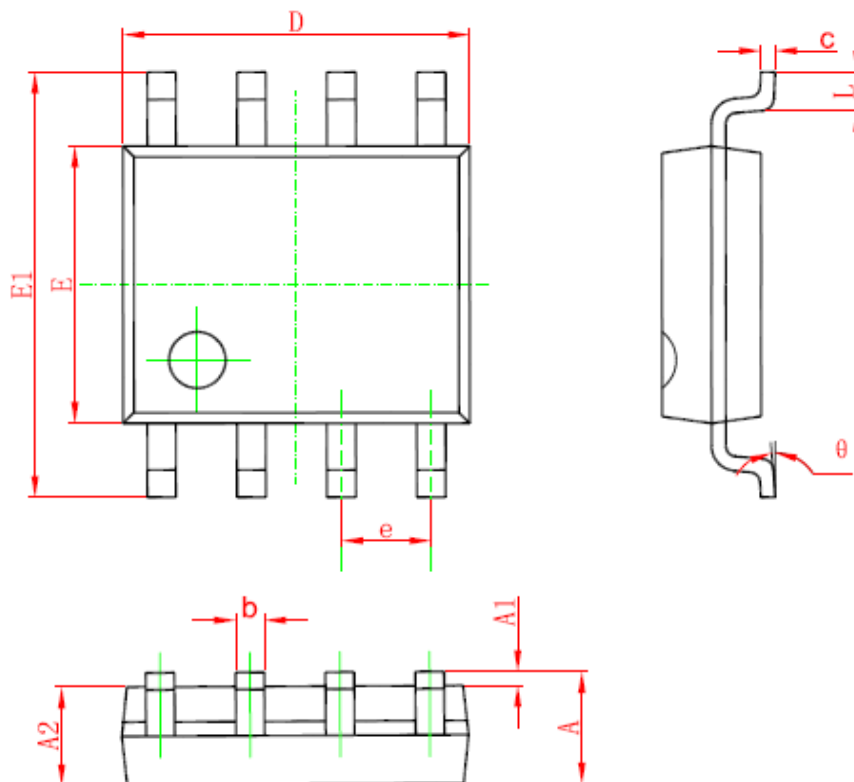
Fig. 11 Unclamped Inductive Waveform



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### SOP-8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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